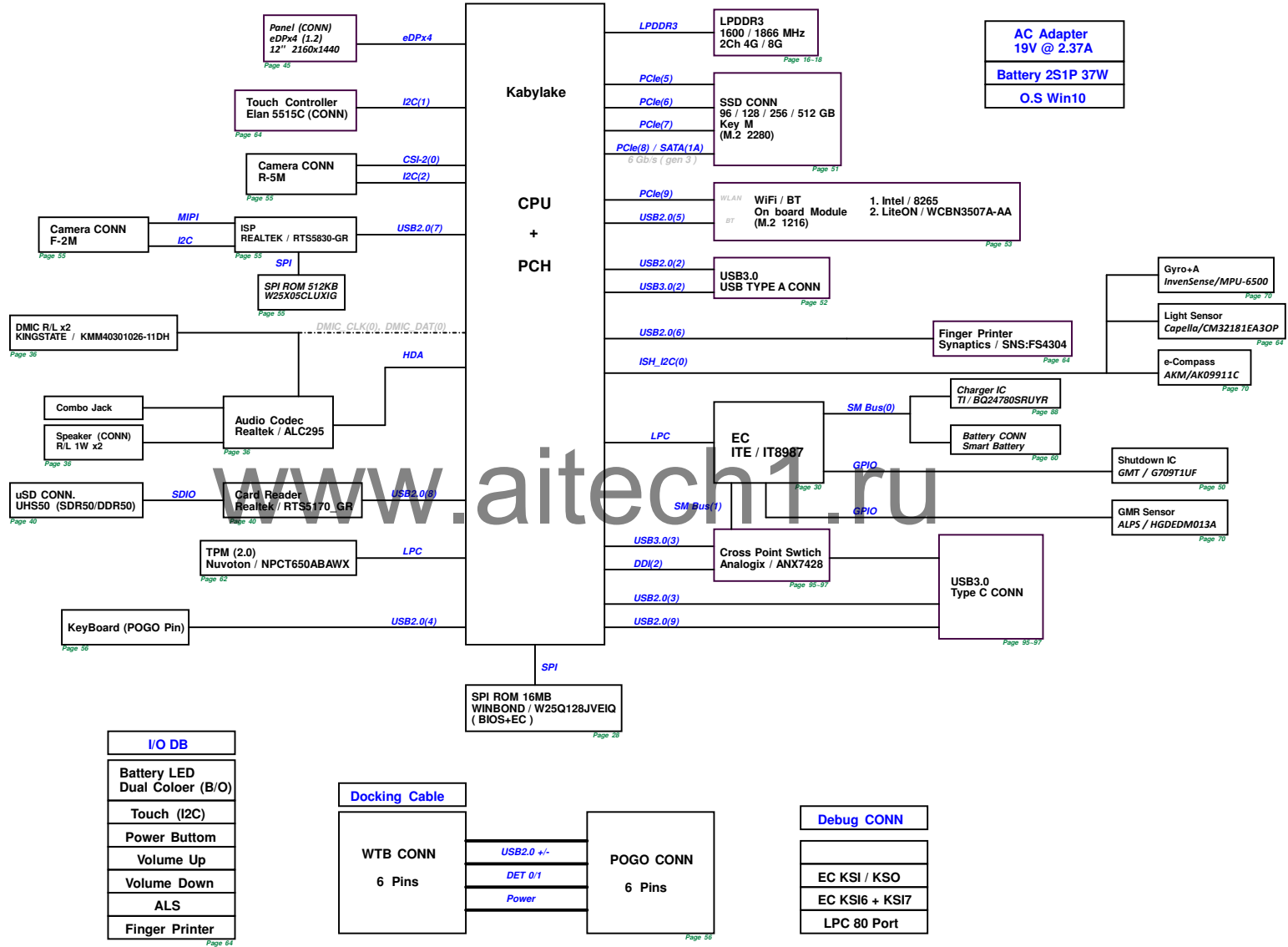


# GUAM BLOCK DIAGRAM

## SYSTEM PAGE REF.

01. Block Diagram  
02. Mount Table  
03. CPU(1)\_DDI / eDP  
04. CPU(2)\_LPDDR3  
05. CPU(3)\_+VCCORE  
06. CPU(4)\_+VCCGT  
07. CPU(5)\_+VDDQ/IO/SA  
08. CPU(6)\_CPU GND  
09. CPU(7)\_CFG/RSVD  
16. LPDDR3(1)\_MEMORY DOWN  
17. LPDDR3(2)\_MEMORY DOWN  
18. LPDDR3(3)\_CA/DQ Voltage  
20. PCH(1)\_SPI / LPC  
21. PCH(2)\_ISH / GPIO / I2C  
22. PCH(3)\_HDA / DMIC / SDIO  
23. PCH(4)\_USB / PCIE / SATA  
24. PCH(5)\_CLK / RTC / CSI-2  
25. PCH(6)\_POWER MANAGEMENT  
26. PCH(7)\_POWER  
28. PCH(9)\_SPI / SMB  
30. EC\_IT8987  
32. RST\_Reset Circuit  
36. Codec / Jack / SpK / DMIC  
40. CR\_RTS5170 / Micro SD  
41. ISH CONN  
44. Debug CONN  
45. LCM\_EDP  
50. THERMAL / NUT  
51. SSD NGFF  
52. USB 3.0 TYPE-A CONN  
53. WLAN / BT M.2 1216  
55. Camera 2M / 5M  
56. IO CONN / POGO PIN  
57. Discharge  
60. DC\_DC / BAT CONN  
62. TPM  
68. BYPASS EC SEQUENCE  
69. Finger printer  
70. Sensor / GMR  
80. POWER\_VCORE for U22  
81\_POWER\_SYSTEM  
82\_POWER\_+1.0VSUS  
83\_POWER\_DDR & VTT\_UMA  
84\_POWER\_1.8VSUS  
88\_POWER\_CHARGER  
89\_POWER\_AC\_PD\_WC Input  
90\_POWER\_DETECT  
91\_POWER\_LOAD\_SWITCH  
92\_POWER\_PROTECT  
93\_POWER\_SIGNAL  
94\_POWER\_FLOWCHART  
95\_USB\_TYPE-C ANX7428  
96\_USB\_TYPE-C Receptacle  
97\_USB\_TYPE-C Dead Bat tery  
A01. Power Tree  
B01. IO Board



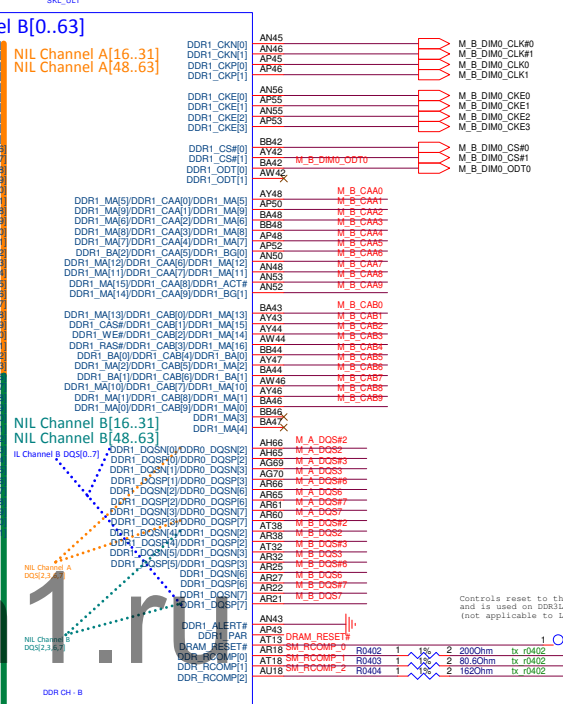
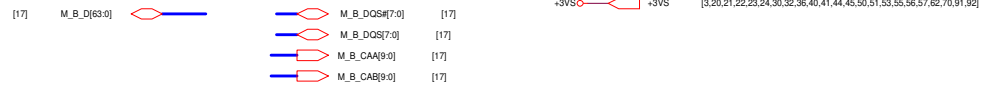
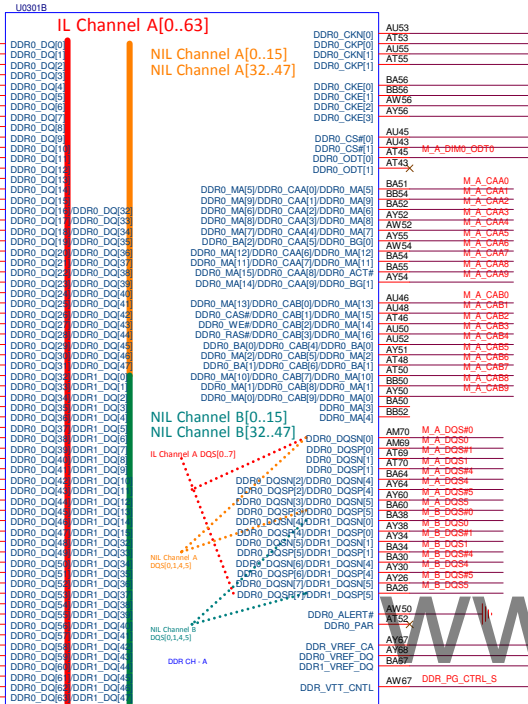
## Mount Table

Optional	Mount?
/MEM-CH1	V
/MEM-CH2	V
/TPM	V
/Debug	V
/NON-IOAC	V
/USBSLP	X
/IOAC	X
/SEQS_EC	X
/BYPAS_EC	V
/DB	X
/NON-DB	X
/VG_BOM	X
/NON-vPro	V
/vPro	X

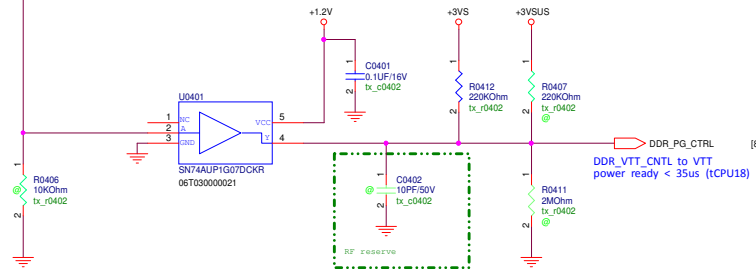
AVAP	
Audio Codec	N-AV-nonAP
LAN	N/A
Antenna	Y (Not include WiGig Antenna)
Touchpad (Click Pad)	Y
3G/LTE	N/A
TPM	N-AV-nonAP
IMR	N/A
Sensor hub	N
Gyro sensors	Y
G sensors	Y
eCompass	Y
Proximity sensor	N/A
Light Sensor(ALS)	Y
EC	N
PMIC	N/A
GPS	N/A
Touch IC	Y
Padding	N
Keyboard	Y
IME	Y(TBD)
Other AVAP	A cover and U frame (TBD)
B&S	
CPU	Y
Chipset	N/A
VRAM	N/A
SSD/HDD	Y
System MEM	Y
Panel	Y
Touch Sensor	Y
Battery	Y
Adapter	Y
Camera	Y
WLAN/BT	Y
Other B&S 1	
Other B&S 2	
Other B&S 3	
Other B&S 4	



[16]	M_A_D[63:0]			M_A_DQS#[7:0]	[16]
				M_A_DQS[7:0]	[16]
				M_A_CAA[9:0]	[16]
				M_A_CAB[9:0]	[16]



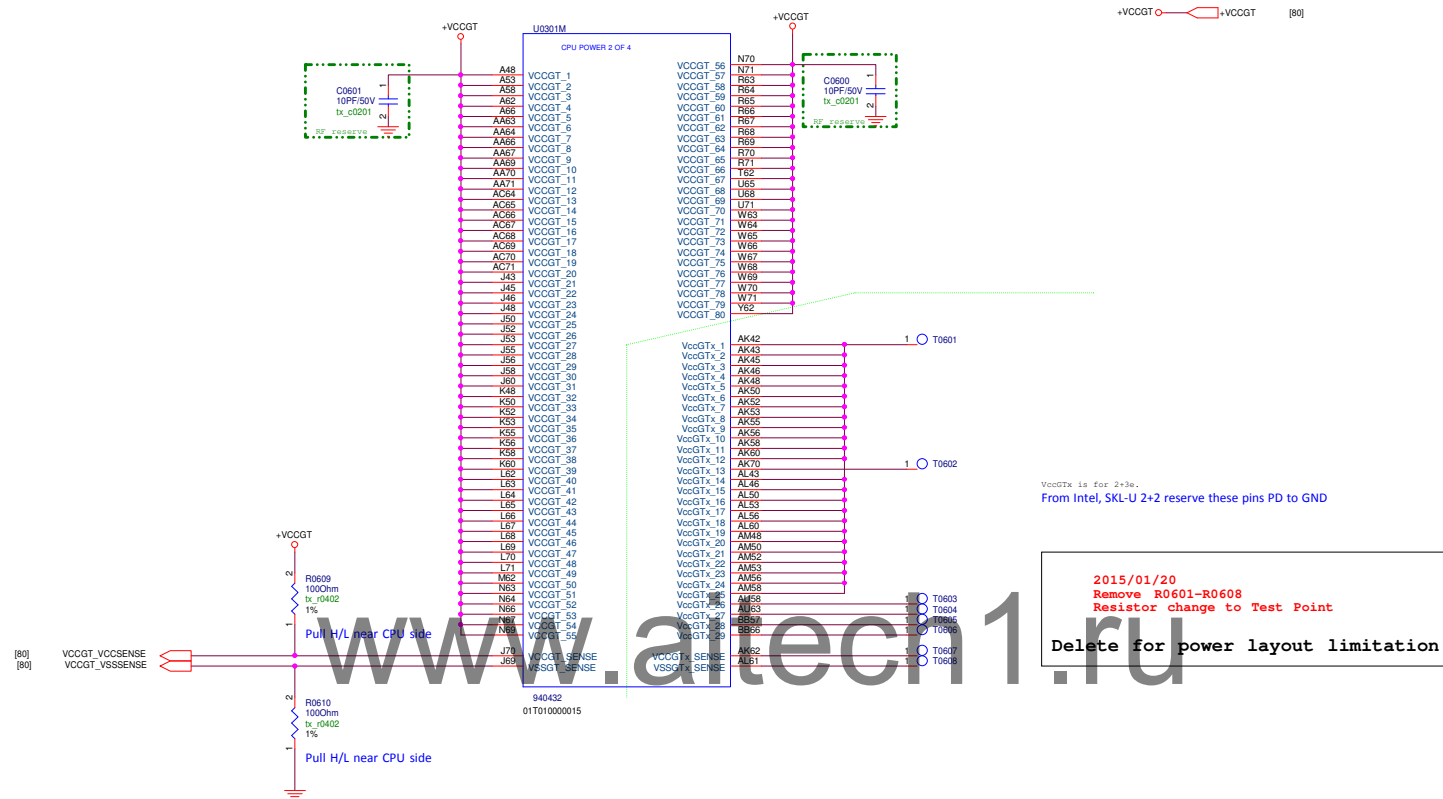
Symbol U0301 B	
	interleaved(Symbol default) Non-interleaved
BYTE 0	ChannelA DQ[0..15] DQS/DQS#[0,1]
BYTE 1	
BYTE 2	ChannelADQ[32..47] DQS/DQS#[4,5]
BYTE 3	ChannelA DQ[0..63] DQS/DQS#[0..7]
BYTE 4	ChannelB DQ[0..15] DQS/DQS#[0,1]
BYTE 5	
BYTE 6	ChannelB DQ[32..47] DQS/DQS#[4,5]
BYTE 7	

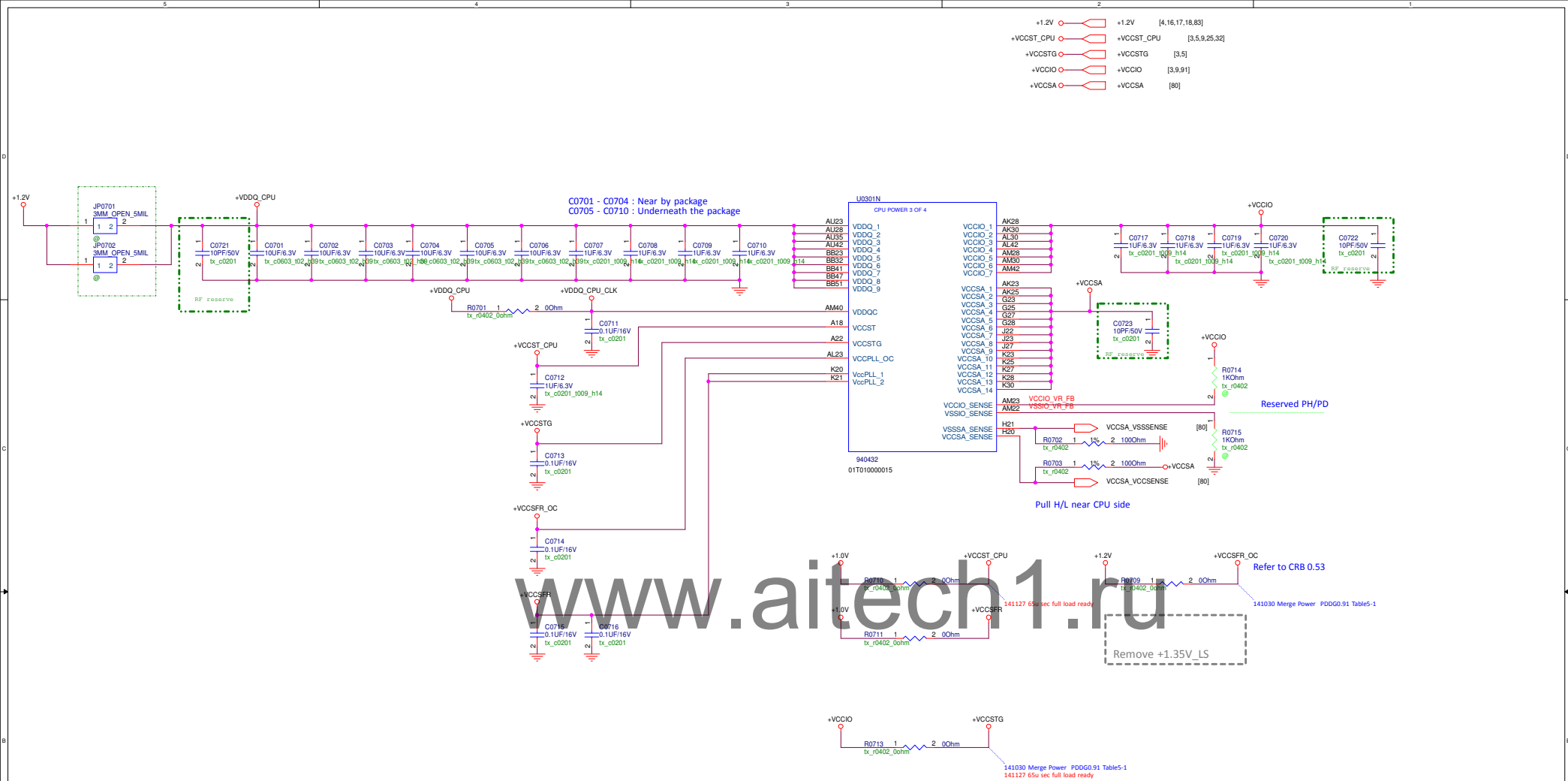


Symbol U0301 C	
	interleaved(Symbol default)
BYTE 0	ChannelB DQ[0..63] DQS/DQS#[0..7]
BYTE 1	
BYTE 2	
BYTE 3	
BYTE 4	
BYTE 5	
BYTE 6	
BYTE 7	
	Non-interleaved
	ChannelA DQ[16..31] DQS/DQS#[2,3]
	ChannelADQ[48..63] DQS/DQS#[6,7]
	ChannelB DQ[16..31] DQS/DQS#[2,3]
	ChannelB DQ[48..63] DQS/DQS#[6,7]







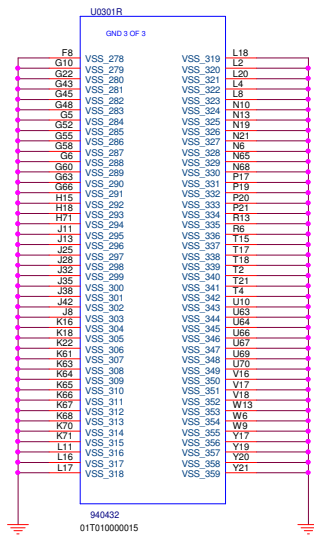
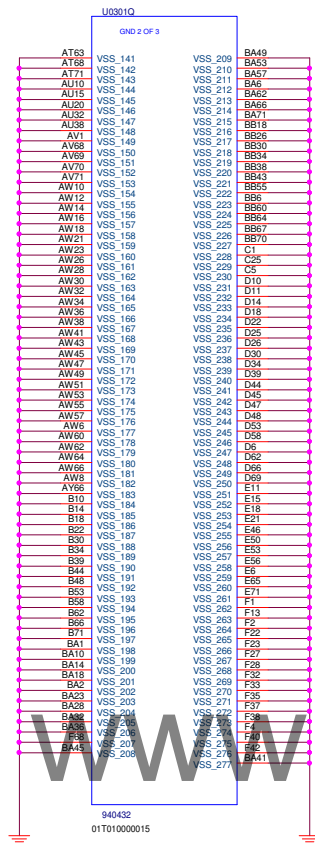
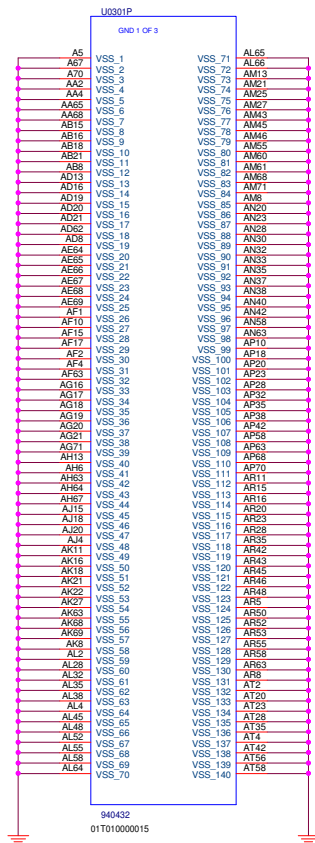


**Table 5-1. Power Rail Requirements – Volume Segment – U-Line**

Load switch (LS)	LS ENABLE	Load/Rail name	Imax (A)
<= 65usec full load ready (Note 16)	SLP_S4#	VCC <sub>ST</sub>	0.04
		VCC <sub>PLL</sub> (VCC <sub>SFR</sub> )	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VCC <sub>IO</sub>	3.0
		VCC <sub>STG</sub>	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically Tcpu\_04

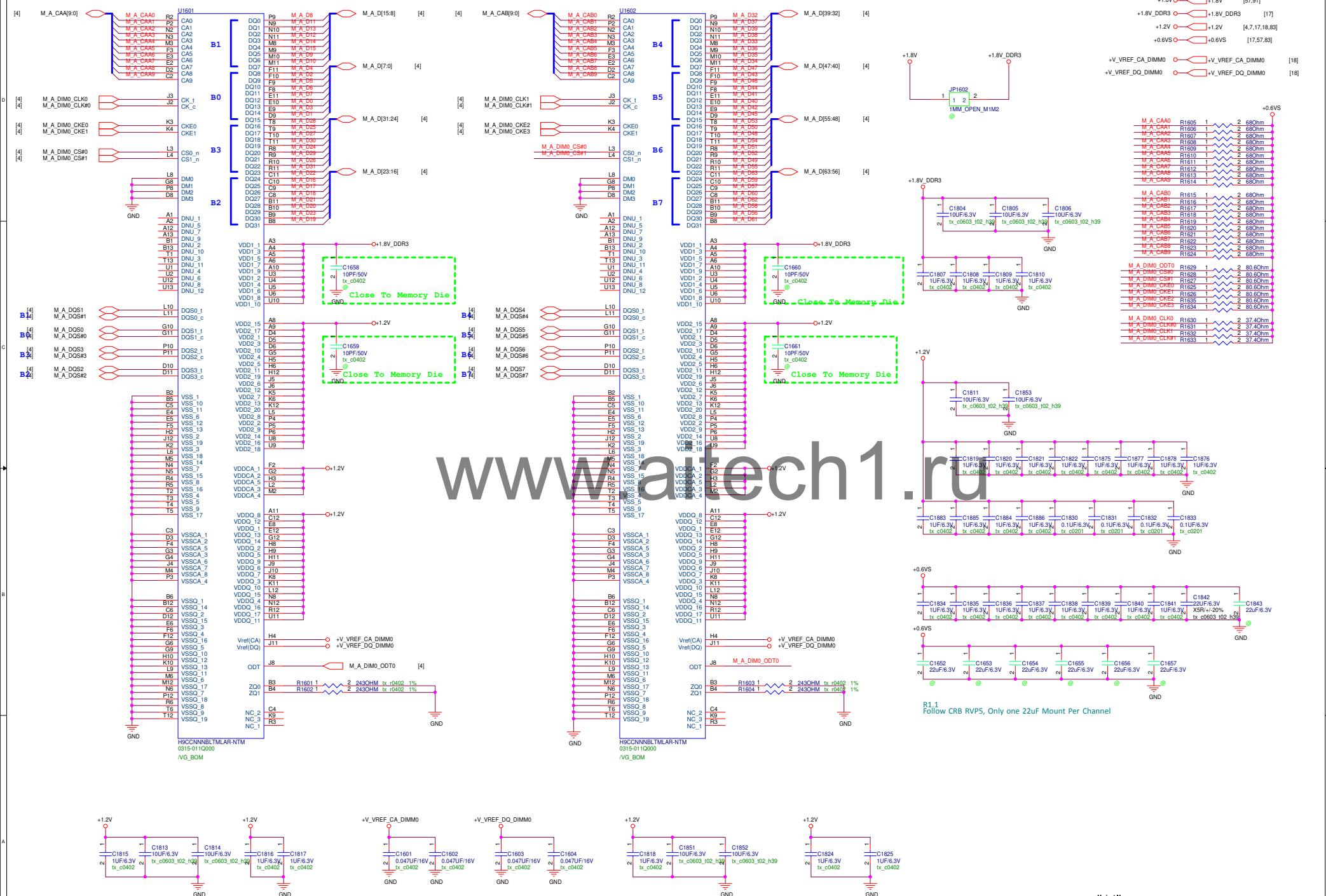
reference 543977\_543977\_SKL\_PDDG\_Rev0\_91



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LPDDR3 Channel A



&lt;Variant Name&gt;

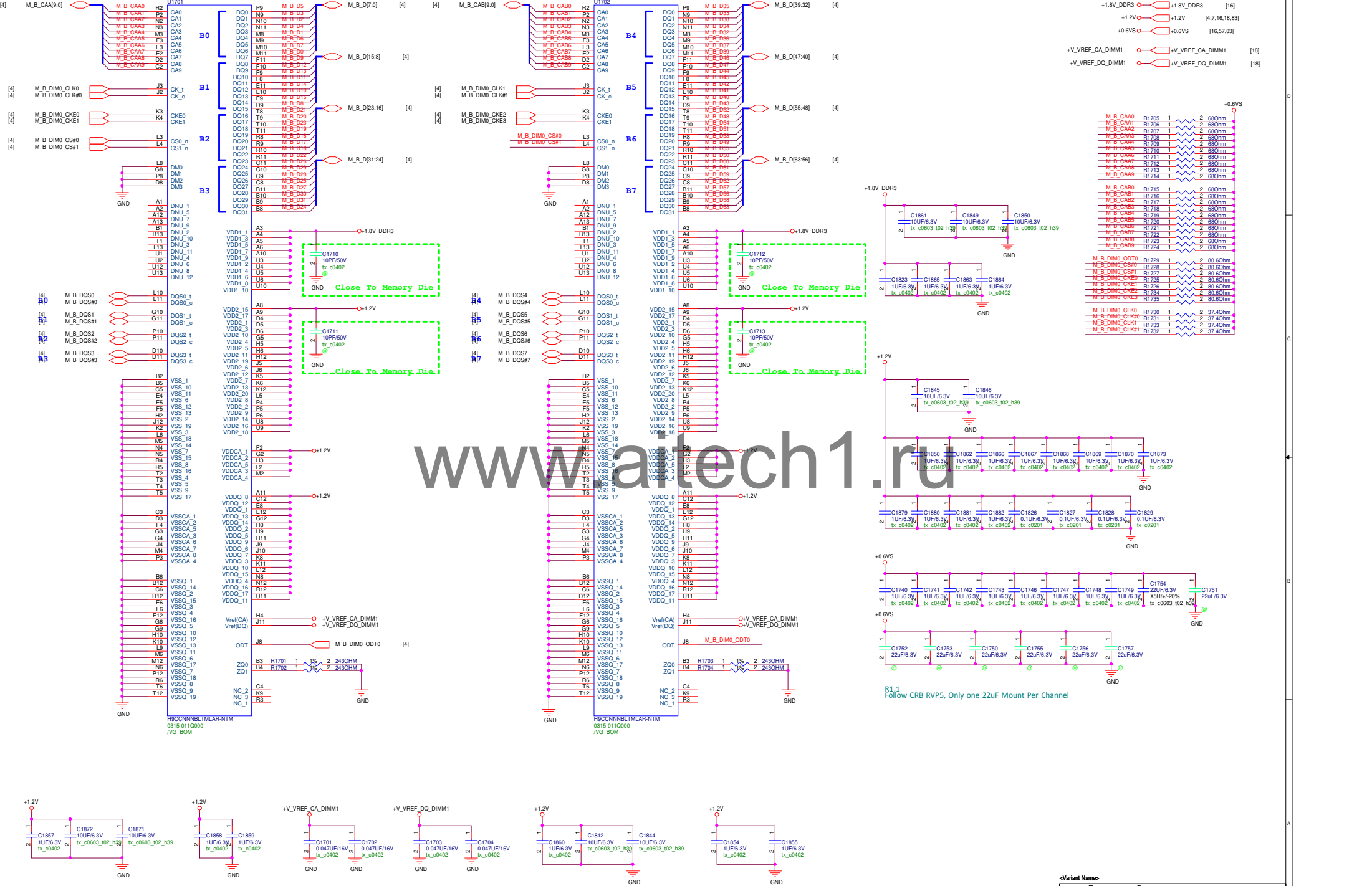
**PEGATRON** Title LPDDR3(1) Channel A

Engineer: *Willy Liang*

Size	Project Name	Re
C	GUAM	0.0

Date: Wednesday, March 15, 2017 Sheet 16 of 100

LPDDR3 Channel B





# LPDDR3 Vref

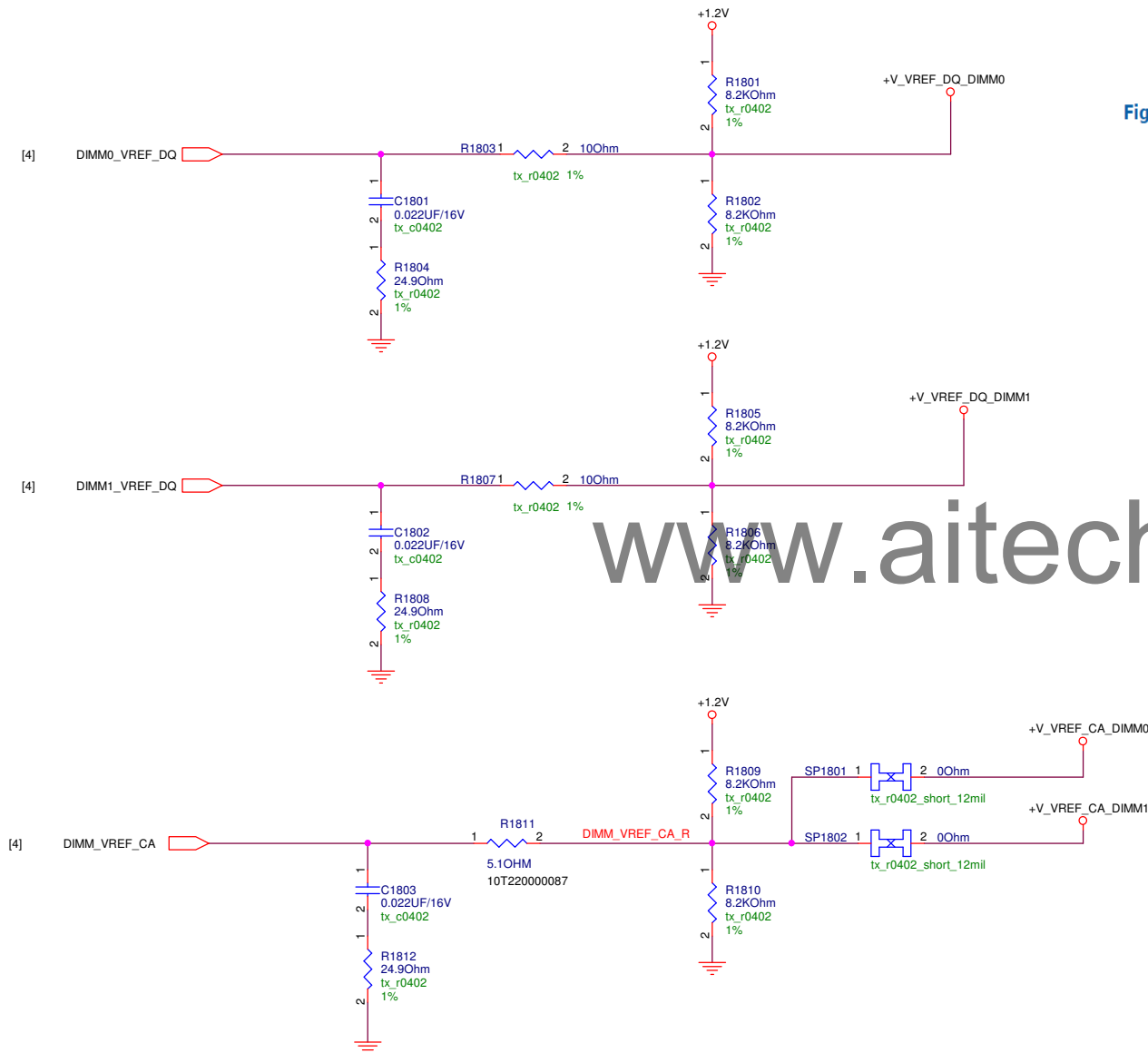
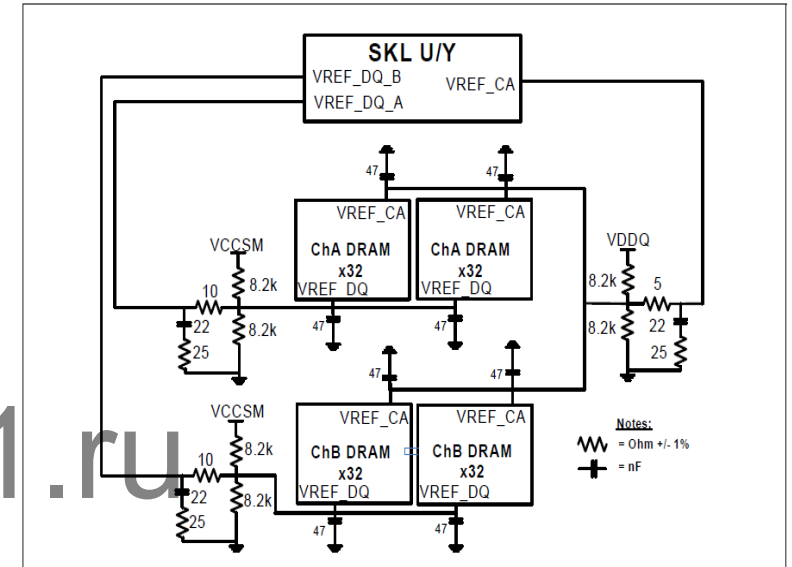
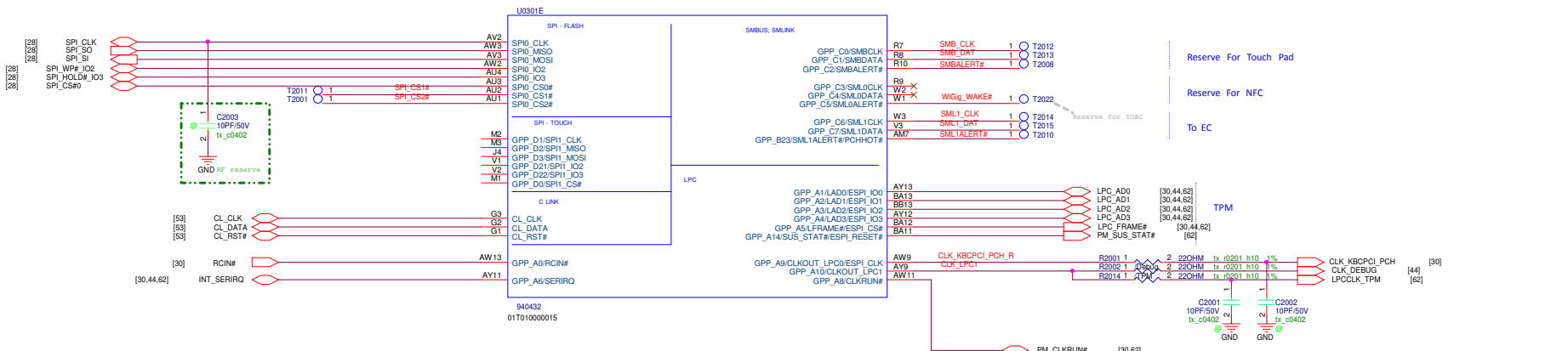
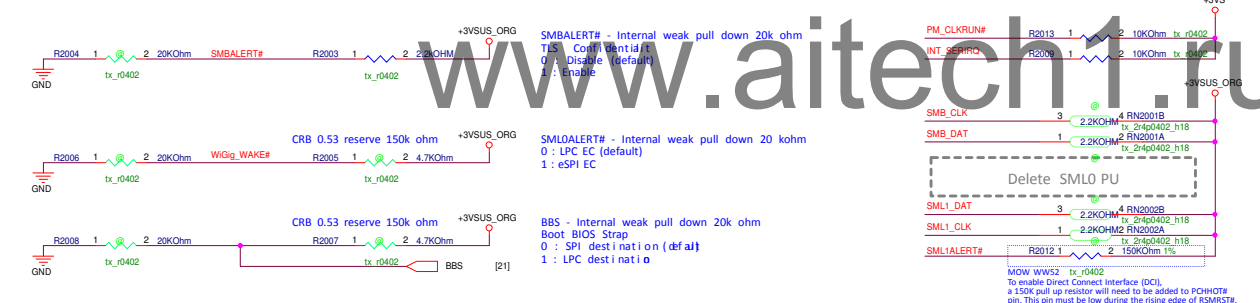


Figure 4-46. SKL U and SKL Y LPDDR3 x32 Memory Down V<sub>REF-DQ</sub> and V<sub>REF-CA</sub> Overview

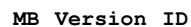
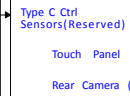
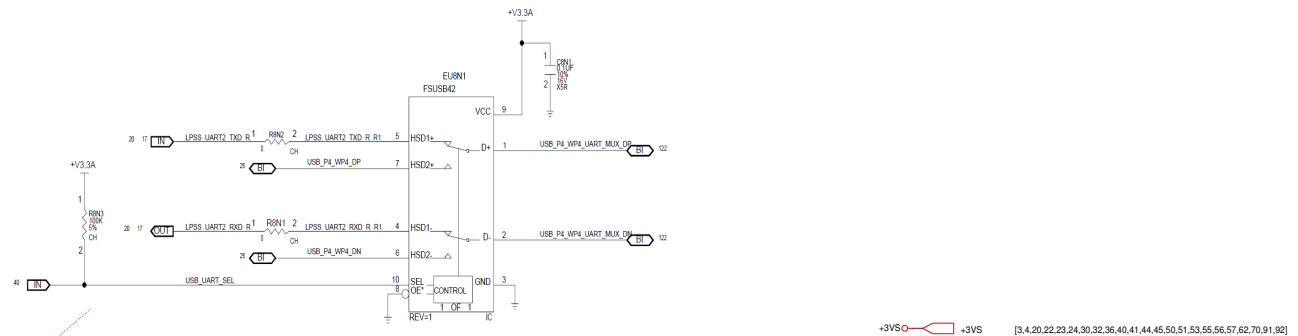
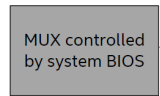
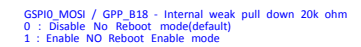
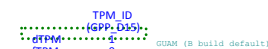




Unmount R2013,R2009  
Vendor Suggest Pull High Resistor Need To Close To TPM  
PM\_CLKRUN#, INT\_SERIRQ Need To Pull 10kohm To+3VS at Chipset Side



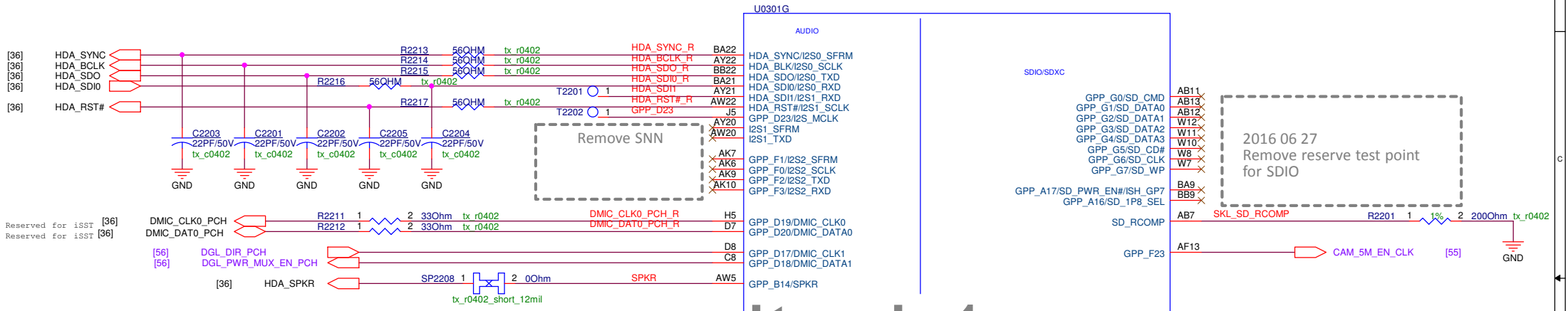
## With skylake EHCI Removal, Potential Gap with Windows\* 7 Kernel Debug and OS Installation - Mitigation Required

Memory IDTPM ID

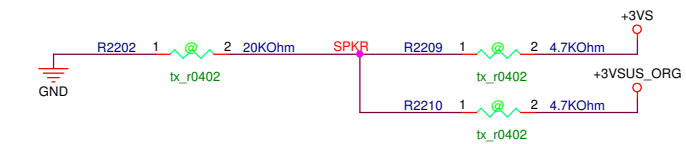
Default is GPO, to reserve pull high to +3VSUS\_ORG

**PEGATRON** Title : **PCH(2)\_ISH**  
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4		Engineer: <u>Willy_Liao</u>	
Size C	Project Name <b>GUAM</b>	Rev 0.0	
Date: <u>Wednesday, March 15, 2017</u>		Sheet <u>21</u> of <u>100</u>	

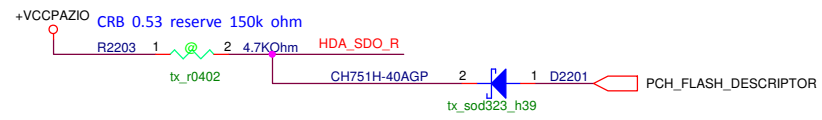


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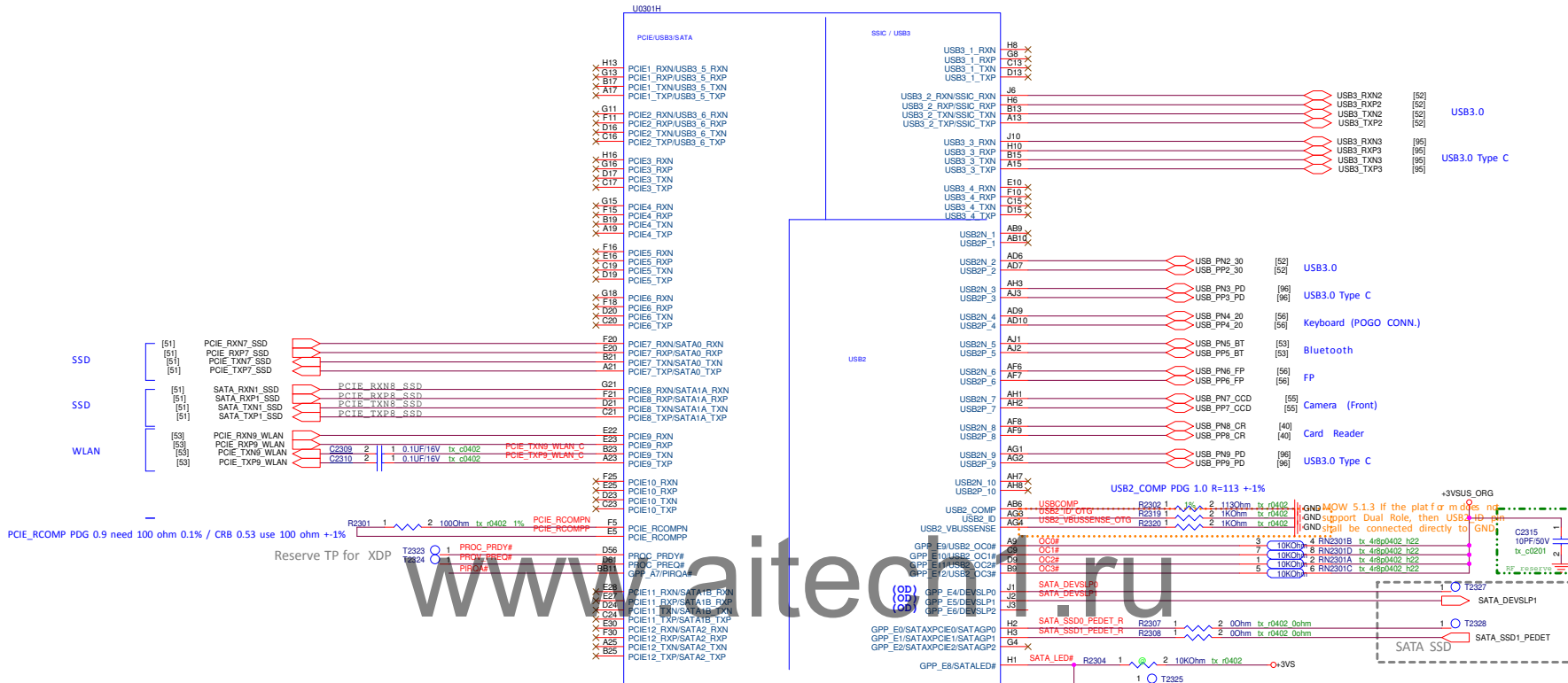
SPKR - Internal weak pull down  
0 : Disable TOP Swap mode (default)  
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS\_ORG



HDA\_SDO - Internal weak pull down  
0 : Enable security measure defined in the Flash Descriptor  
1 : Disable Flash Descriptor Security

<b>PEGATRON</b>		<b>Title : PCH(3)_HDA/SDIO</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1-NB4</b>		<b>Engineer: Willy_Liao</b>	
Size <b>B</b>	Project Name <b>GUAM</b>		Rev <b>0.0</b>
Date: <b>Wednesday, March 15, 2017</b>		Sheet <b>22</b> of <b>100</b>	



**Table 1-2. PCH-LP SKUs (Sheet 2 of 2)**

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express <sup>1</sup> Storage Devices	0	2	2

**Notes:**

1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

**Table 1-3. PCH-LP HSIO Detail**

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Base-U	USB 3.0/SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe
Premium-U	USB 3.0/SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe
Premium-Y	USB 3.0/SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe

Capture from 545659\_545659\_SKL\_PCH\_LP\_EDS\_Rev1.0\_pub  
Please refer the latest Doc.

### 3.4.1 SKL PCH U Flexible I/O

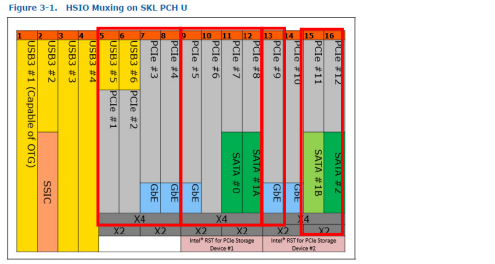
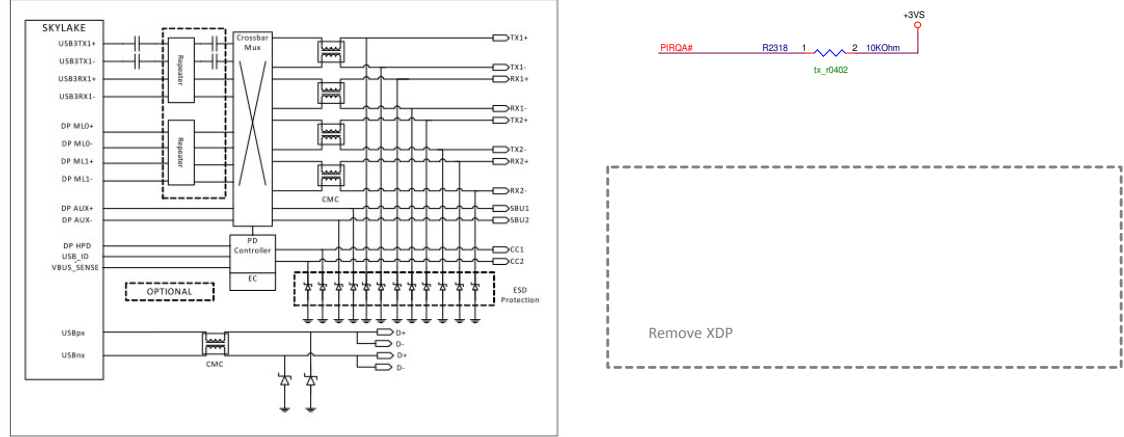
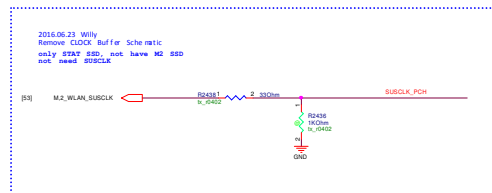
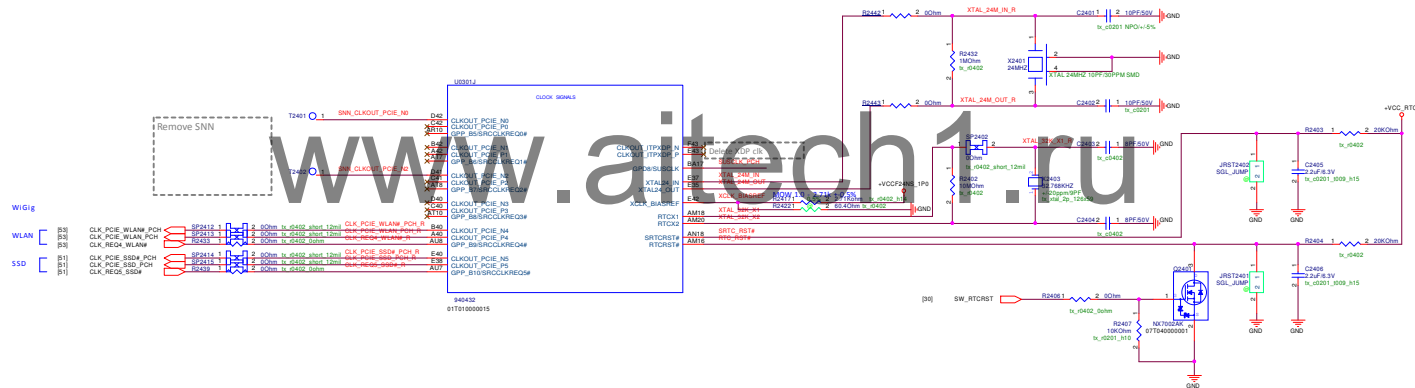


Figure 16-18.USB 3.0 Dual Role and DP x 2



**Note:** The figure above is a high level example implementation block; actual implementation on schematic may vary.



<b>PEGATRON</b>		Title	<b>PCH(S)_CLK</b>
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BD1-MB4		Engineer:	<i>Willy_Liao</i>
Size	Project Name		Rev
D	<b>GUAM</b>		0.0
Date: Wednesday, March 15, 2017		Sheet	24 of 100





Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

U30310

CPU POWER 4 of 4

0.696V AB19  
AB20  
P18

2.5744V AF18  
AF19  
V20  
V21

0.0224V K17  
L1

0.0884V N15  
N16  
N17  
P15  
P16

0.0264V K15  
L15

0.1184V V15  
AB17  
Y18

0.0684V AD17  
AD18  
AJ17

0.0314V AJ19  
AJ16

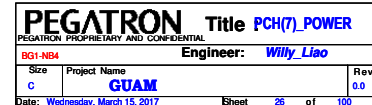
0.6474V AF20  
AF21  
T10  
T20

0.1475V AJ21

0.696V AK20

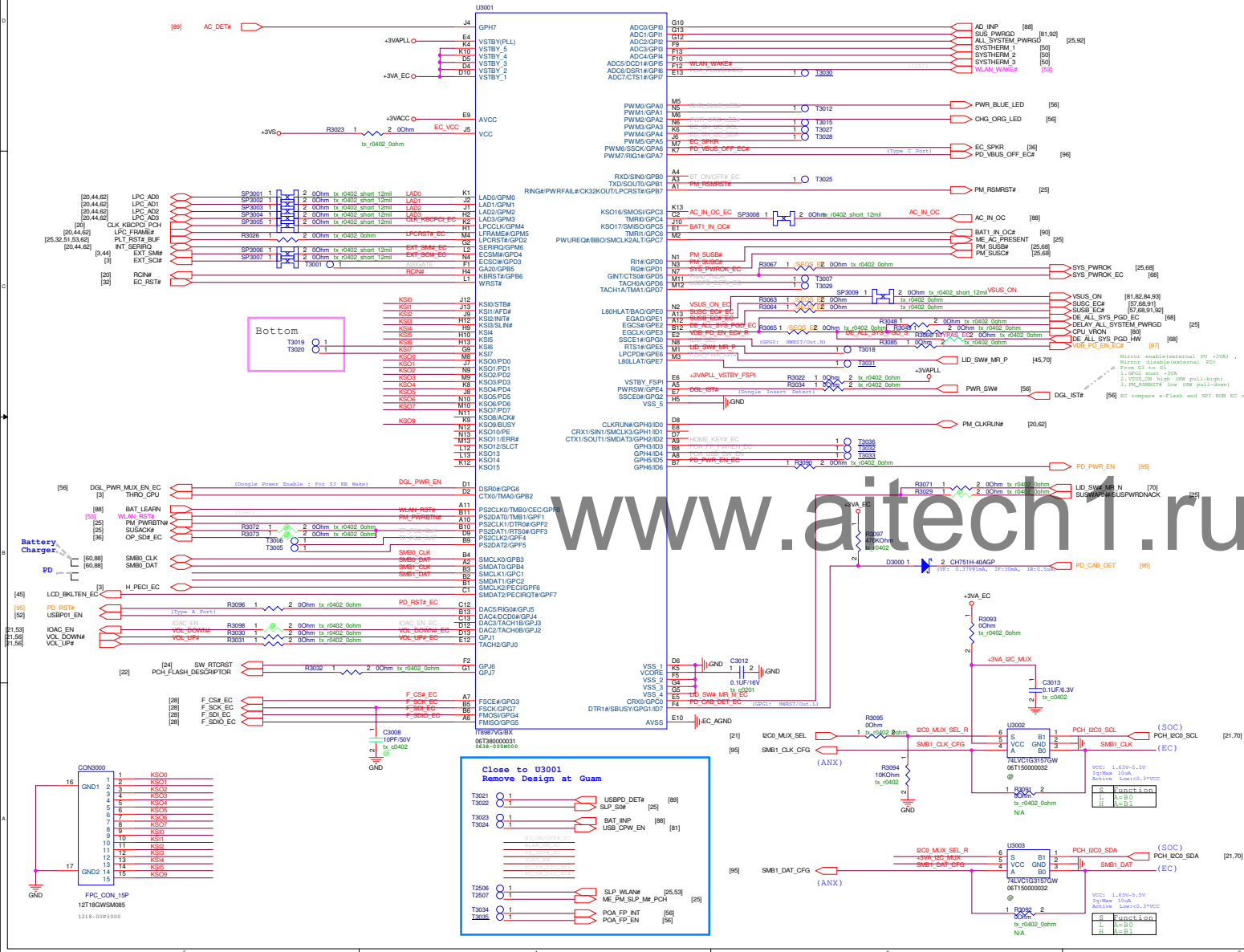
0.0334V N18

VCCPRIM\_1P0\_1  
VCCPRIM\_1P0\_2  
VCCPRIM\_1P0\_3  
VCCPRIM\_CORE\_1  
VCCPRIM\_CORE\_2  
VCCPRIM\_CORE\_3  
VCCPRIM\_CORE\_4  
DCPDSW\_1p0  
VCCMPHYAON\_1P0\_1  
VCCMPHYAON\_1P0\_2  
VCCMPHYGT\_1P0\_1  
VCCMPHYGT\_1P0\_2  
VCCMPHYGT\_1P0\_3  
VCCMPHYGT\_1P0\_4  
VCCMPHYGT\_1P0\_5  
VOCAMPHYPLL\_1P0\_1  
VOCAMPHYPLL\_1P0\_2  
VOCAPLL\_1P0  
VCCPRIM\_1P0\_4  
VCCPRIM\_1P0\_5  
VCCDSW\_3p3\_1  
VCCDSW\_3p3\_2  
VCCDSW\_3p3\_3  
VCOHDA  
VCCSPI  
VCCSRAM\_1P0\_1  
VCCSRAM\_1P0\_2  
VCCSRAM\_1P0\_3  
VCCSRAM\_1P0\_4  
VCCSRAM\_3p3\_1  
VCCPRIM\_1P0\_6  
VCCPRIM\_1P0\_7  
VCCPRIM\_1P0\_8  
VCCPRIM\_1P0\_9  
VCCPRIM\_1P0\_10  
VCCPRIM\_1P0\_11  
VCCPRIM\_1P0\_12  
VCCPRIM\_1P0\_13  
VCCPRIM\_1P0\_14  
VCCPRIM\_1P0\_15  
VCCPRIM\_1P0\_16  
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VCCPRIM\_1P0\_22  
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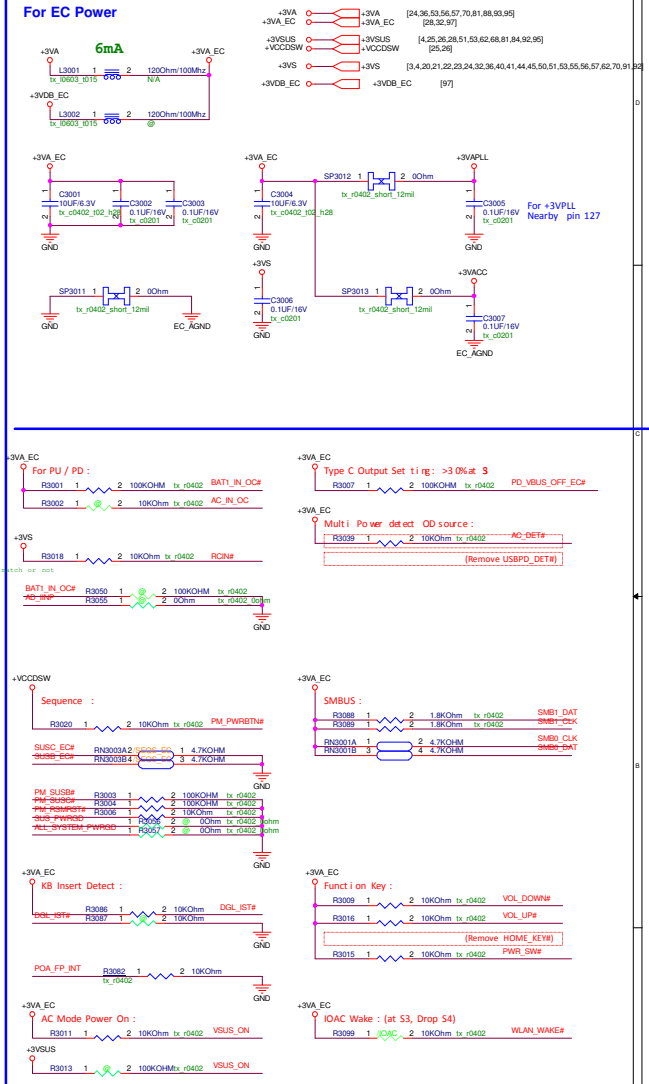


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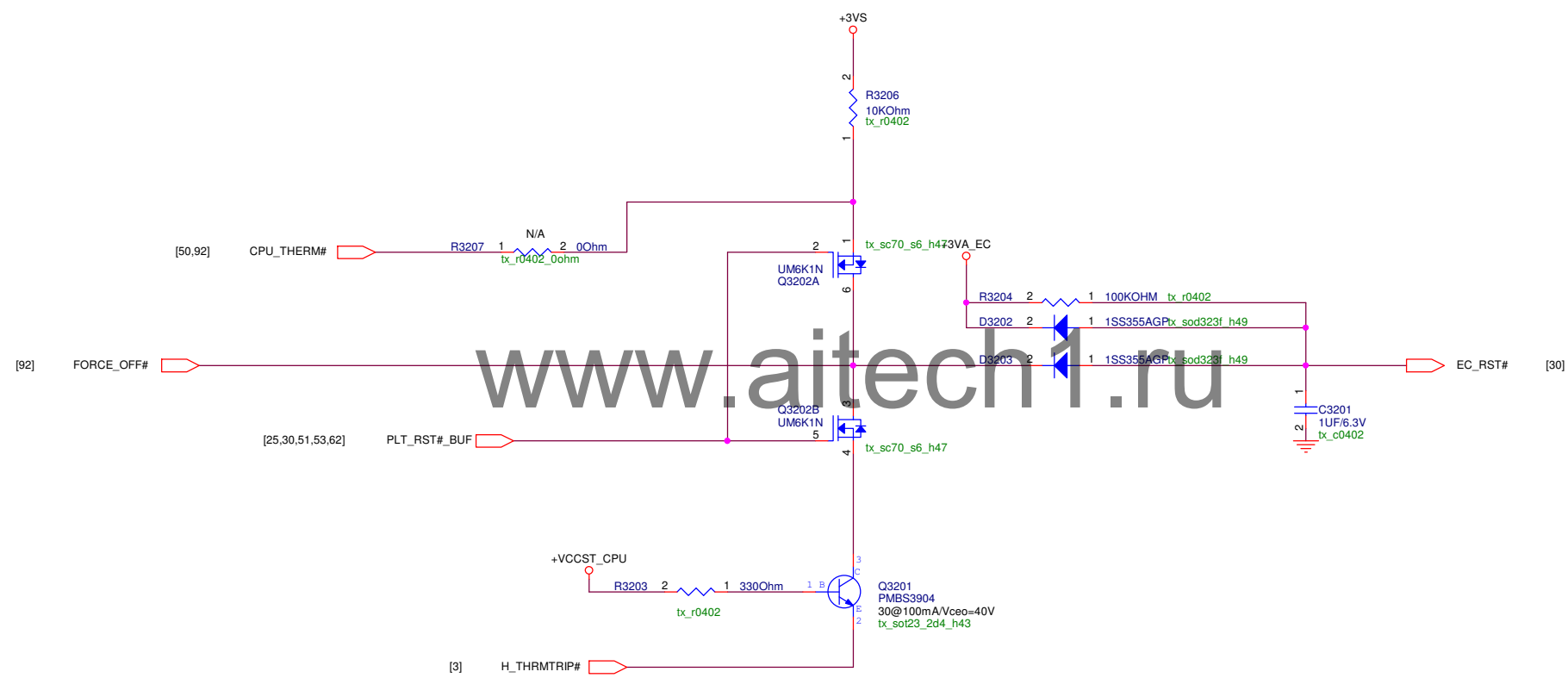
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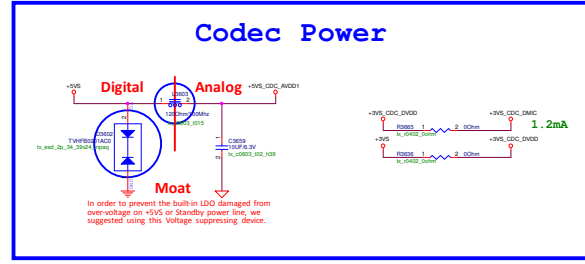
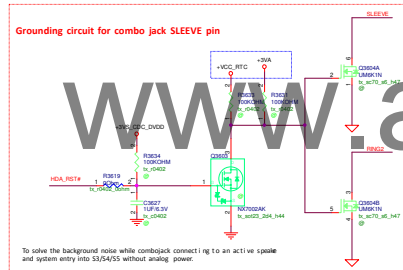
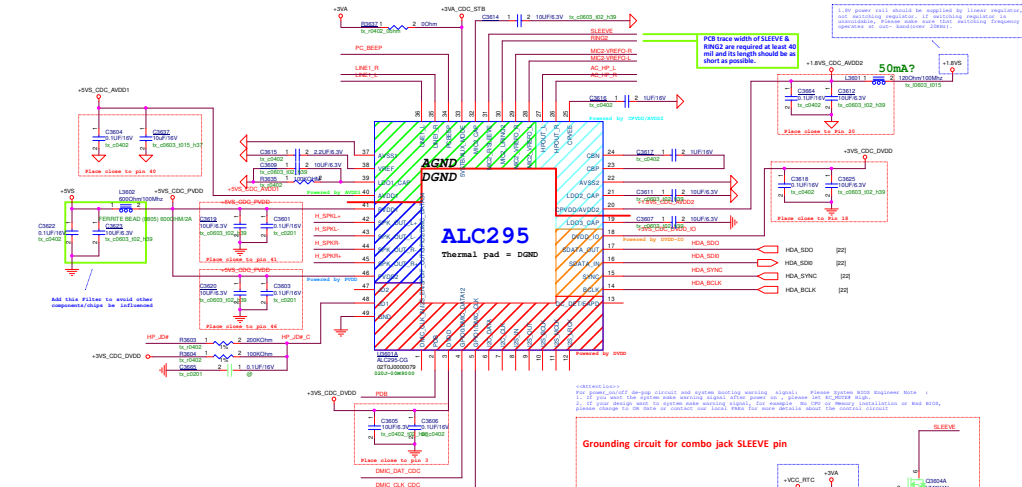
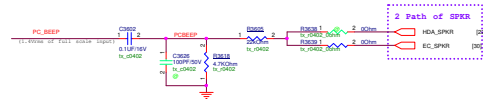
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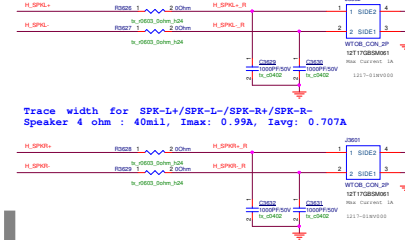
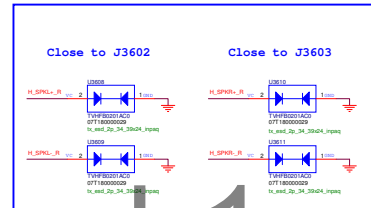
+VCCST\_CPU [3,5,7,9,25]  
+3VA\_EC [28,30,97]  
+3VS [3,4,20,21,22,23,24,30,36,40,41,44,45,50,51,53,55,56,57,62,70,91,92]



# Audio Codec

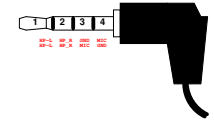


## Internal Speaker R/L

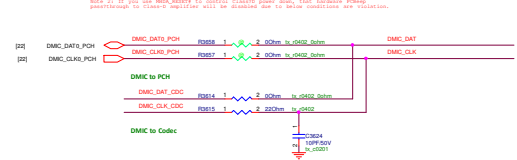


## Universal Audio Jack

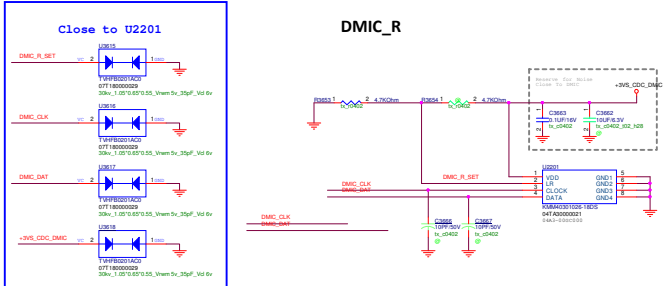
(OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input)  
 PCB trace width of (SLEEVE)/RING2 are required at least 40 mil  
 for HP crossstalk consideration and, its length should be as short as possible.  
 L3607/L3608 should choose DC resistance (Rdc) < 30m-ohm  
 to get the best audio performance for HP crossstalk.



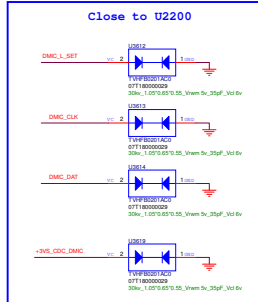
## DMIC



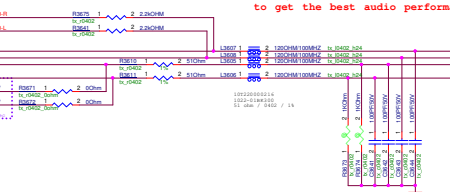
## DMIC\_R



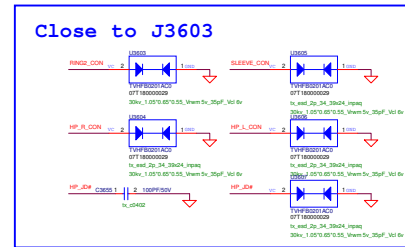
## DMIC\_L



## DMIC\_L



## Close to J3603

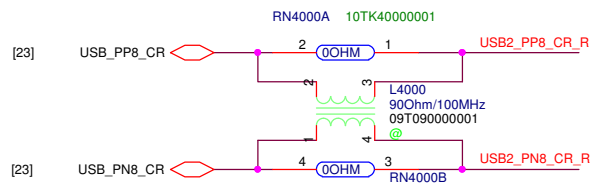
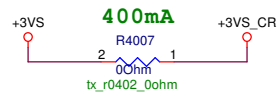


Part Number	Vrwm (Reverse Stand-Off Voltage)	CL (Any I/O pin to GND)	Hawaii
07T180000029	5.5V (max)	22pF (max) / 17.5pF (typ)	no used
0718-01RG000	5.0V (max)	35pF (max)	no used
0718-01CG000	5.0V (max)	35pF (max)	no used

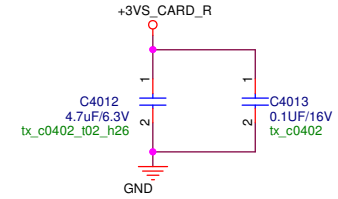
# Card Reader

+3VS [3,4,20,21,22,23,24,30,32,36,41,44,45,50,51,53,55,56,57,62,70,91,92]

## Power Source

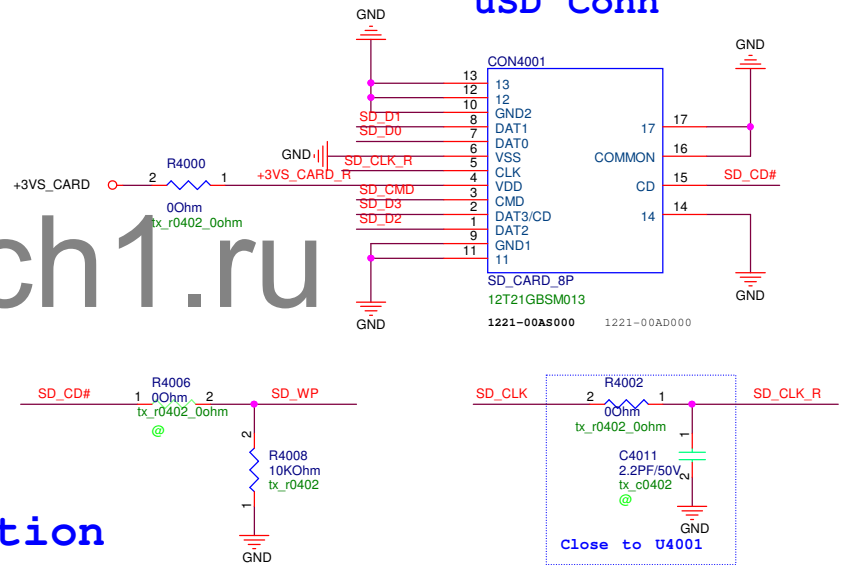


## SD Power

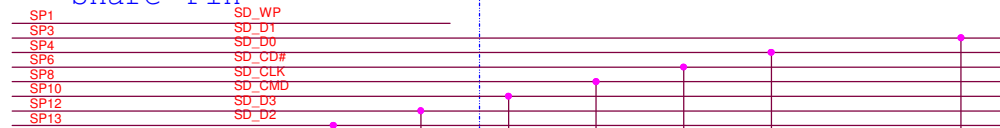


Close to connector CON4001 Pin4

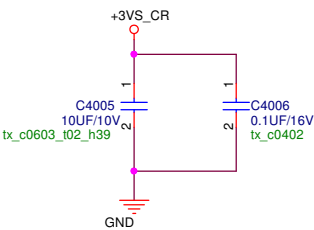
## uSD Conn



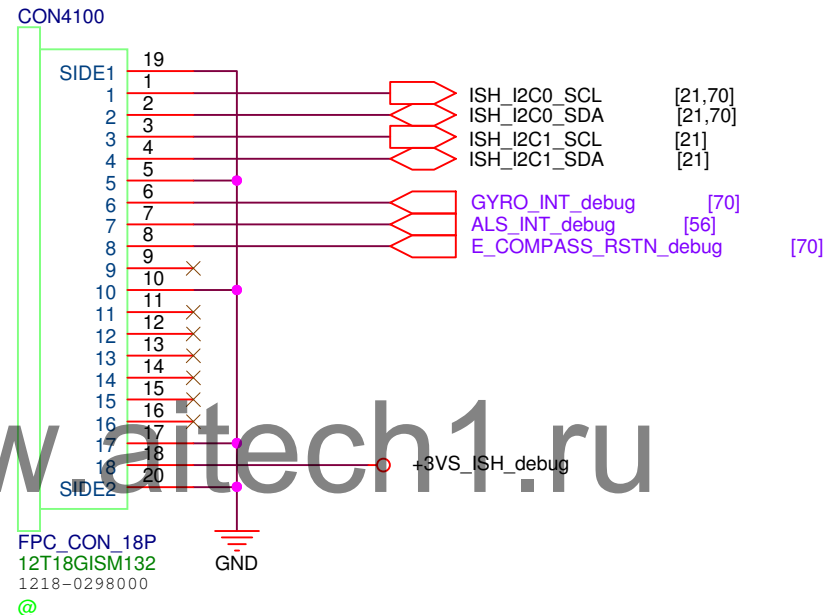
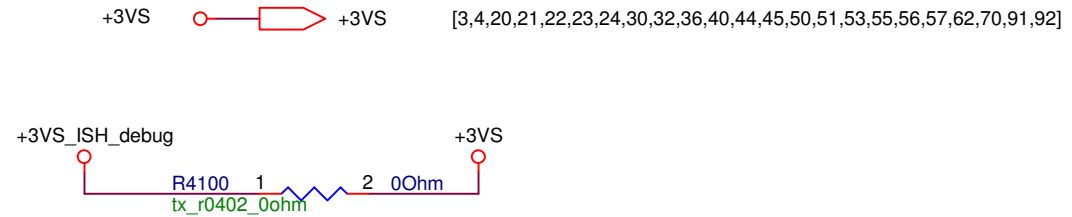
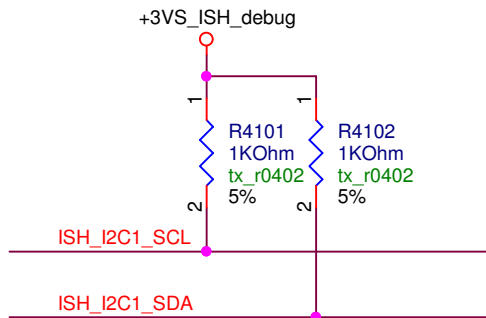
## Share Pin



## ESD solution



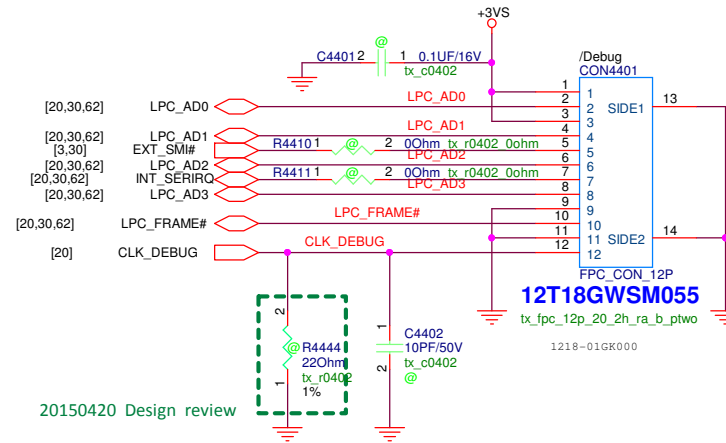
<Variant Name>		Title : Card Reader / uSD	
PEGATRON PROPRIETARY AND CONFIDENTIAL		Engineer: Willy_Liao	
Size B	Project Name	Rev 1.0	
GUAM			
Date: Wednesday, March 15, 2017	Sheet	40	of 100



<b>PEGATRON</b>		Title : ISH debug port	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		Willy_Liao	
Size	Project Name	Rev	
A	GUAM	0.0	
Date: Wednesday, March 15, 2017		Sheet	41 of 100



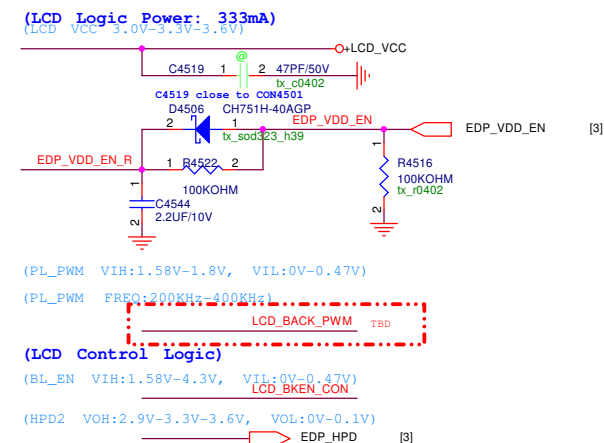
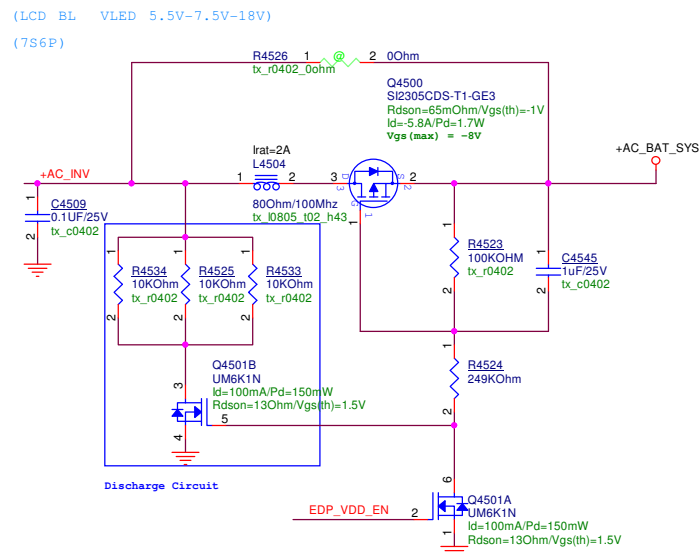
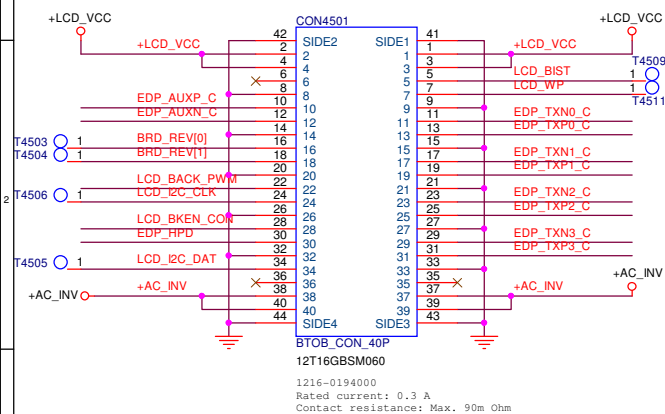
# DEBUG CARD CONN.



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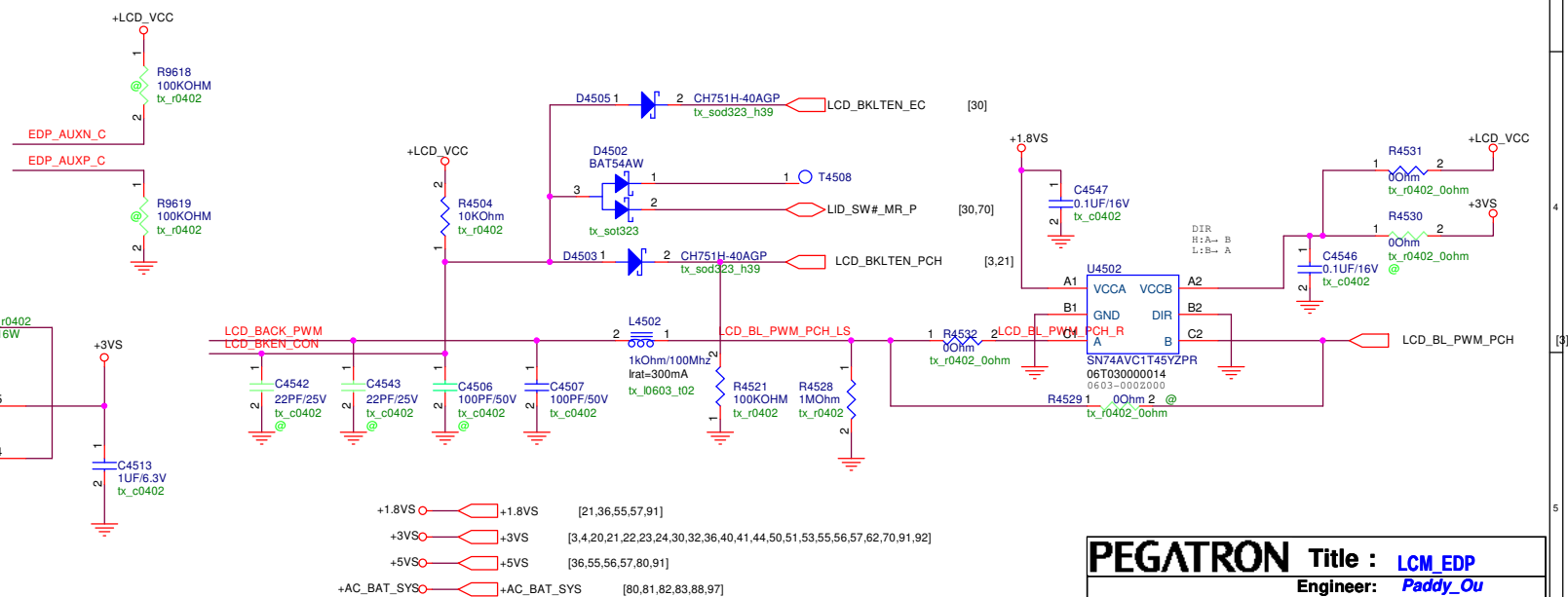
<b>PEGATRON</b>		Title : <b>DEBUG CONN.</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1-NB4</b>		Engineer: <b>Willy_Liao</b>	
Size <b>B</b>	Project Name <b>GUAM</b>		Rev <b>0.0</b>
Date: <b>Wednesday, March 15, 2017</b>		Sheet <b>44</b> of <b>100</b>	

## eDP

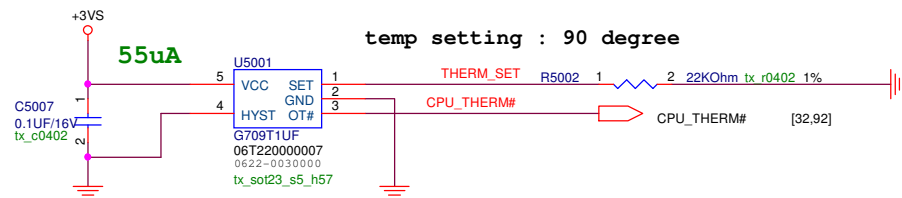


(LCD eDP 1.3 I/F)									
	EDP_AUXP_C	C4510	1	2	0.1Uf/16V	tx_c0402		EDP_AUXP	[3]
	EDP_AUXN_C	C4515	1	2	0.1Uf/16V	tx_c0402		EDP_AUXN	[3]
	EDP_TXN3_C	C4538	1	2	0.1Uf/16V	tx_c0402		EDP_TXN3	[3]
	EDP_TXP3_C	C4529	1	2	0.1Uf/16V	tx_c0402		EDP_TXP3	[3]
	EDP_TXN2_C	C4528	1	2	0.1Uf/16V	tx_c0402		EDP_TXN2	[3]
	EDP_TXP2_C	C4527	1	2	0.1Uf/16V	tx_c0402		EDP_TXP2	[3]
	EDP_TXN1_C	C4523	1	2	0.1Uf/16V	tx_c0402		EDP_TXN1	[3]
	EDP_TXP1_C	C4524	1	2	0.1Uf/16V	tx_c0402		EDP_TXP1	[3]
	EDP_TXN0_C	C4521	1	2	0.1Uf/16V	tx_c0402		EDP_TXN0	[3]
	EDP_TXP0_C	C4522	1	2	0.1Uf/16V	tx_c0402		EDP_TXP0	[3]

## LCD VDDEN / +LED\_VCC

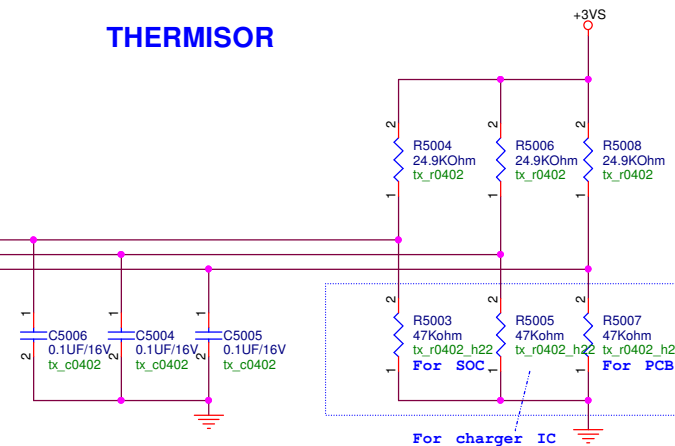


## G709 Thermal Sensor

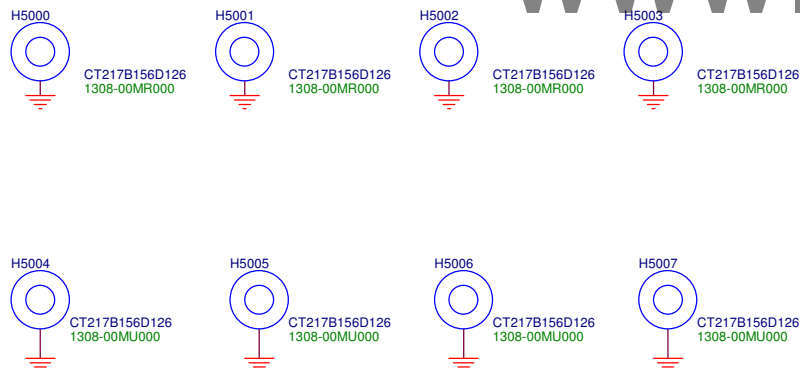


[30] SYSTHERM\_1  
[30] SYSTHERM\_2  
[30] SYSTHERM\_3

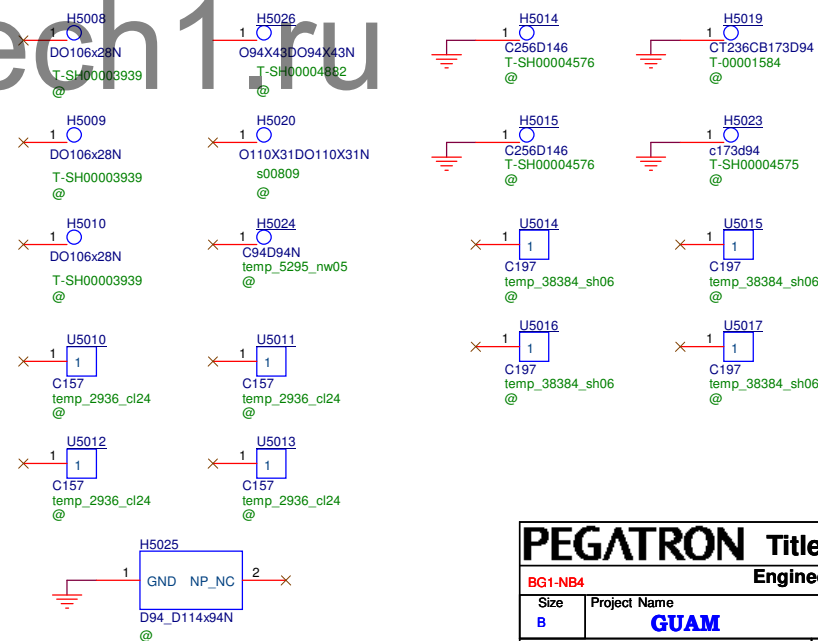
## THERMISOR



## Nut (for CPU)



## Screw Hole / Tooling Hole / SMD PAD



PEGATRON			Title : Thermal/Fan
BG1-NB4			Engineer: Paddy_Ou
Size B	Project Name GUAM		Rev 0.0
Date: Wednesday, March 15, 2017	Sheet	50 of 100	

NGFF socket B -- Main SSD

PCIE\_M\_2\_Electromechanical\_Spec\_Rev\_0\_9-3\_07312013\_RS\_Clean

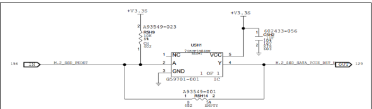
Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes				Module Type and Main Host Interface <sup>1</sup>	Port Configuration <sup>2</sup>
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

36.3.2.3 PEDET Guidelines

PEDET is the interface detect used by PCH to determine the communication protocol that the H.2 card uses; PCIe\* signaling (high) or SATA signaling (low) in conjunction with a platform located pull-up resistor.

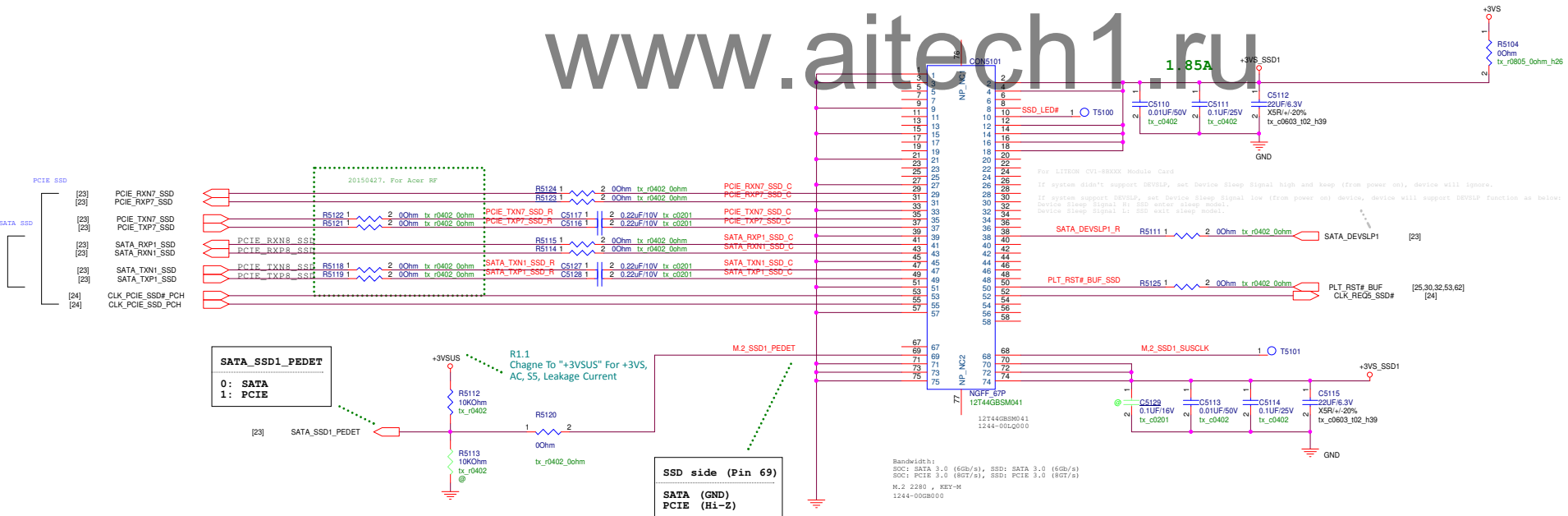
Figure 36-6. PEDET Circuitry Example



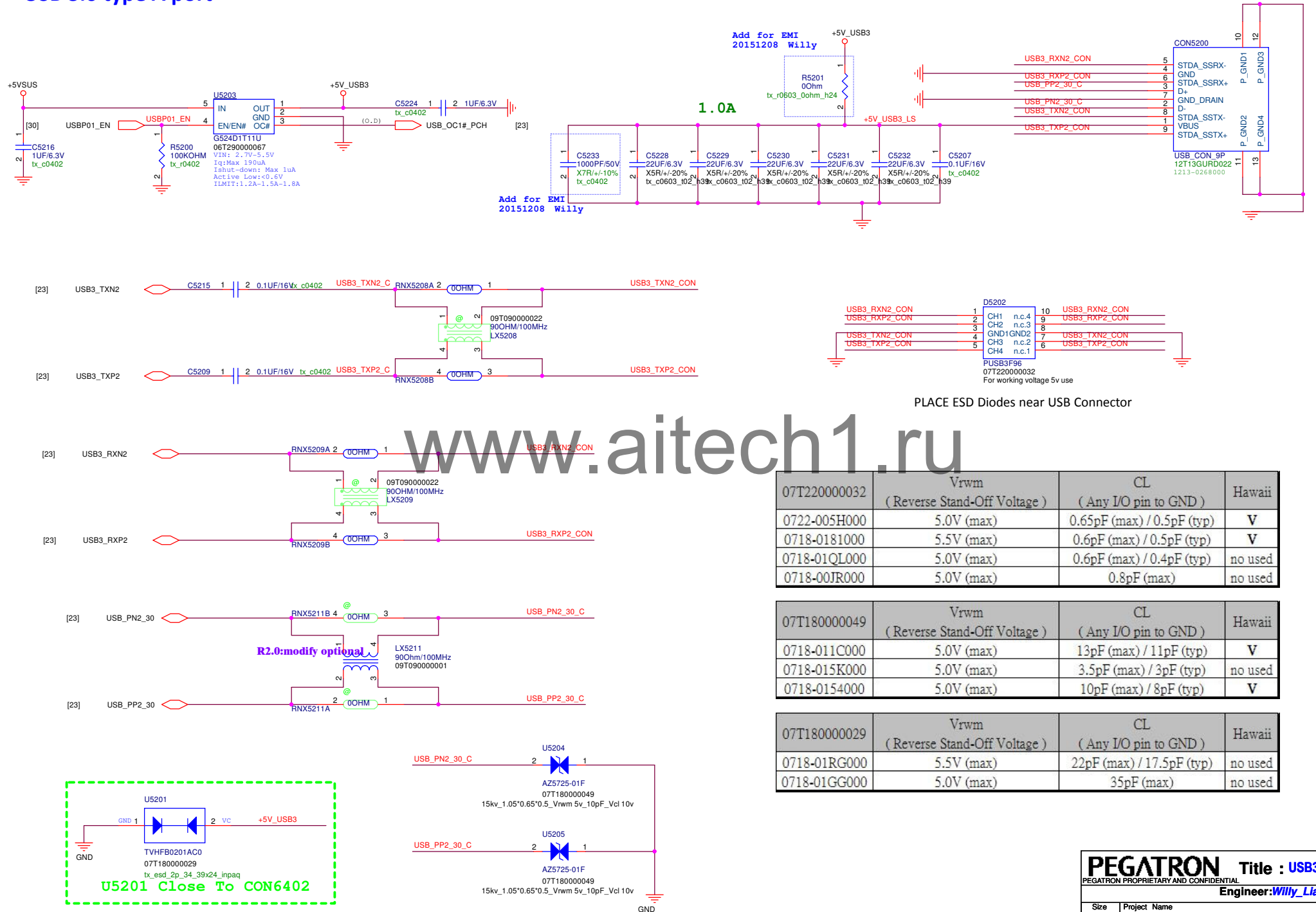
For Skylake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the interface detect signaling from the H.2 device.

2016.06.23 Willy  
Remove For HDD

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# USB 3.0 type A port

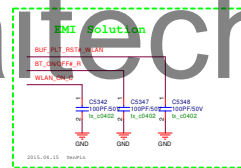
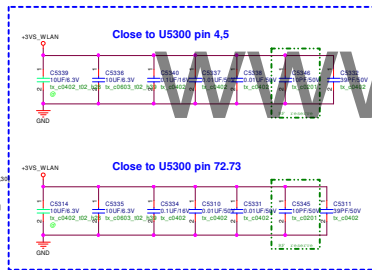
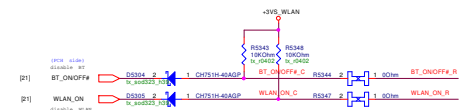
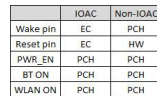


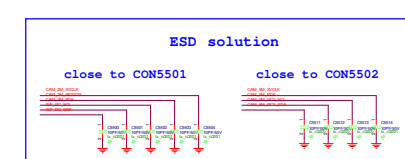
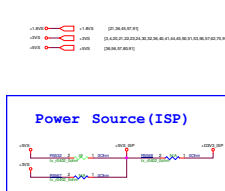
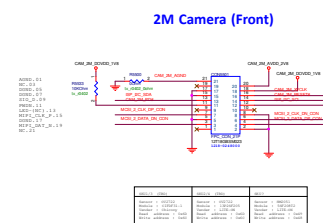
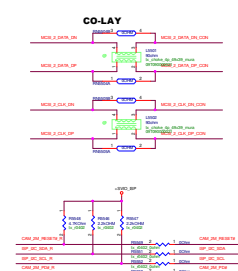
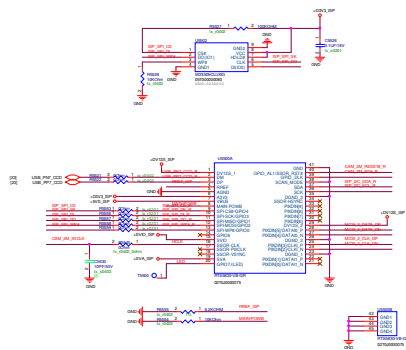
07T220000032	V <sub>rw</sub> m ( Reverse Stand-Off Voltage )	CL ( Any I/O pin to GND )	Hawaii
0722-005H000	5.0V (max)	0.65pF (max) / 0.5pF (typ)	V
0718-0181000	5.5V (max)	0.6pF (max) / 0.5pF (typ)	V
0718-01QL000	5.0V (max)	0.6pF (max) / 0.4pF (typ)	no used
0718-00JR000	5.0V (max)	0.8pF (max)	no used

07T180000049	V <sub>rw</sub> m ( Reverse Stand-Off Voltage )	CL ( Any I/O pin to GND )	Hawaii
0718-011C000	5.0V (max)	13pF (max) / 11pF (typ)	V
0718-015K000	5.0V (max)	3.5pF (max) / 3pF (typ)	no used
0718-0154000	5.0V (max)	10pF (max) / 8pF (typ)	V

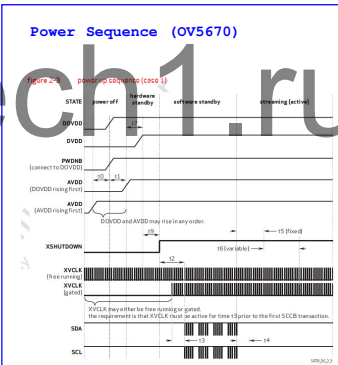
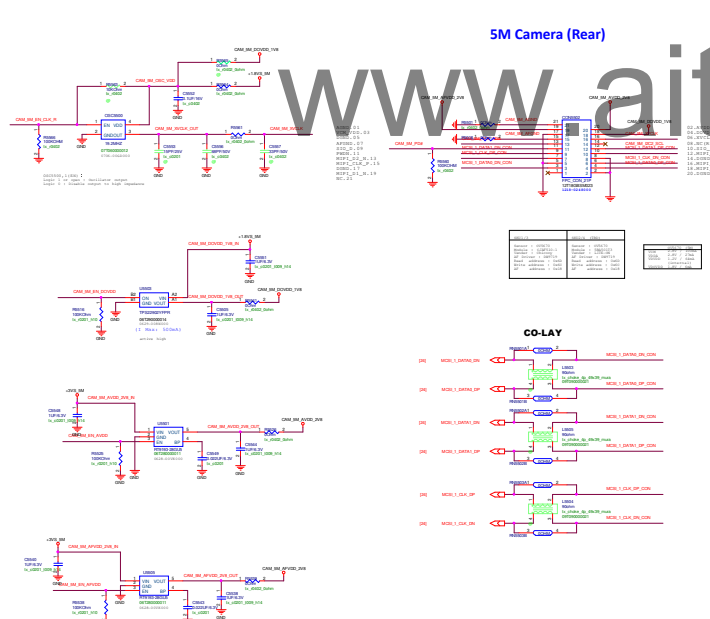
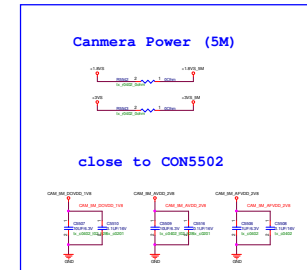
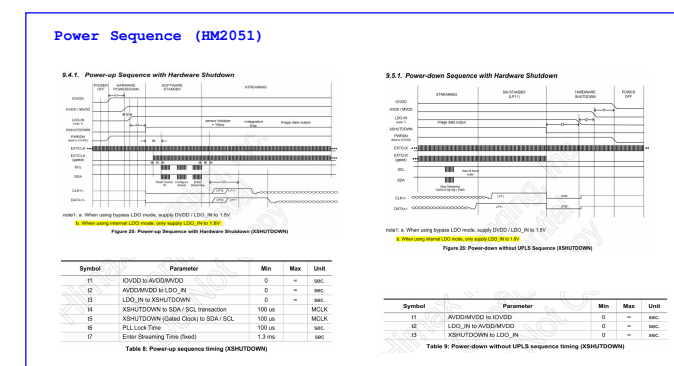
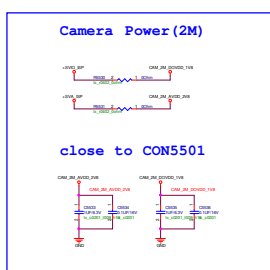
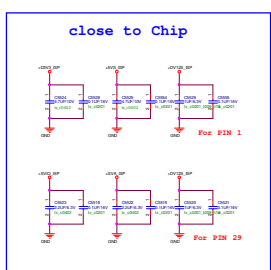
07T180000029	V <sub>rw</sub> m ( Reverse Stand-Off Voltage )	CL ( Any I/O pin to GND )	Hawaii
0718-01RG000	5.5V (max)	22pF (max) / 17.5pF (typ)	no used
0718-01GG000	5.0V (max)	35pF (max)	no used

+3VS  +3VS [3,4,20,21,22,23,24,30,32,36,40,41,44,45,50,51,55,56,57,62,70,91,92]





2016 06 27 Willy  
Remove reserve circuit  
for Camera 2M 2.8V LDO



**table 2-4 power-up sequence timing constraints (sheet 1 of 2)**

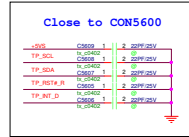
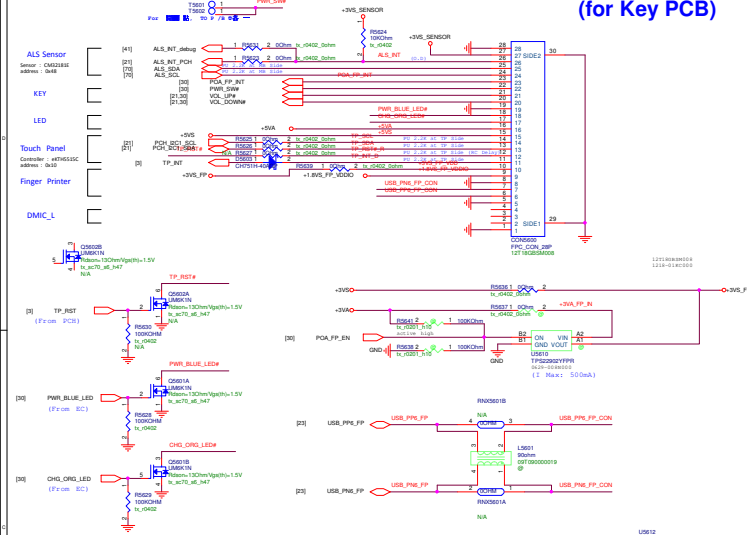
constraint	value	min	max	unit
AVDD rising - DOVDD rising	0	-	900	ns
DOVDD rising - AVDD rising	11	0	-	ns
XSHUTDOWN rising - first SDCB transaction	02	8192	-	XVCLK cycles
sequence number of XVCLK cycles prior to the first SDCB transaction	13	8192	-	XVCLK cycles
PULL start updelay time	14	0.2	ms	
entering streaming mode - first frame start sequence (first part)	15	10	ms	

**table 2-4 power-up sequence timing constraints (sheet 2 of 2)**

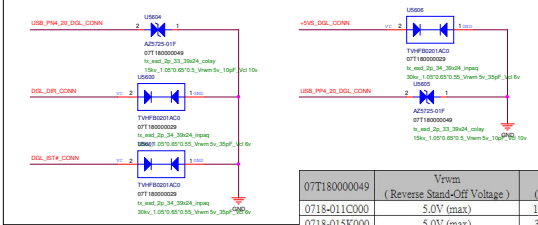
constraint	value	min	max	unit
AVDD or DOVDD, whichever is last - DOVDD	07	0	-	ns
DOVDD - PWDN rising	10	0	-	ns
DOVDD - XSHUTDOWN rising	05	0	-	ns



## FPC connector (for Key PCB)



### Close to CON5601

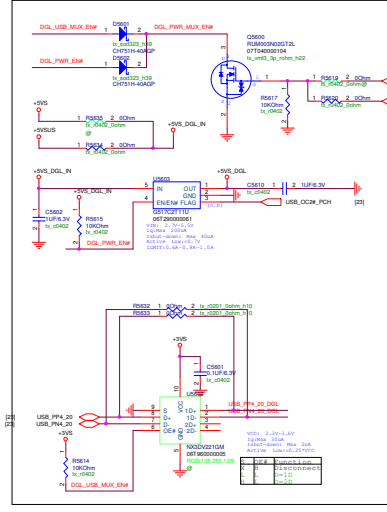


07T180000049	V <sub>revm</sub> (Reverse Stand-Off Voltage)	CL (Any I/O pin to GND)	Hawaii
0718-01C000	5.0V (max)	13pF (max) / 11pF (typ)	V
0718-01S000	5.0V (max)	3.5pF (max) / 3pF (typ)	no used
0718-01S400	5.0V (max)	10pF (max) / 8pF (typ)	V

Step 1: DGL\_1298\_CONN == 0, plug in dock.



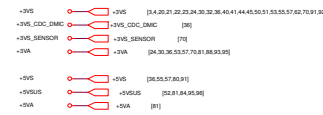
Step 2: Delay 500ms, DGL\_PWL\_MUX\_EN will provide 5V and D+/D-



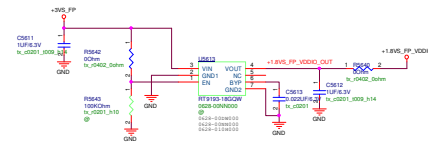
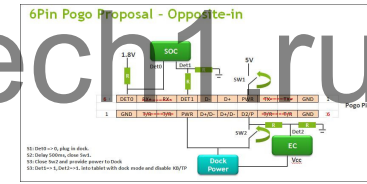
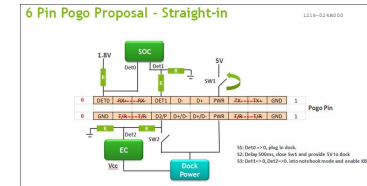
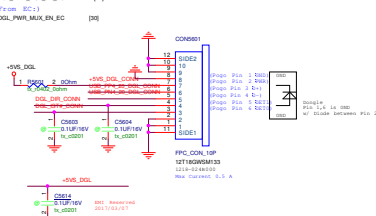
Step 3: DGL\_1298\_CONN == 0, DGL\_SPL\_PCH == 0, into notebook mode



07T180000029	V <sub>revm</sub> (Reverse Stand-Off Voltage)	CL (Any I/O pin to GND)	Hawaii
0718-01RG000	5.5V (max)	22pF (max) / 17.5pF (typ)	no used
0718-01GG000	5.0V (max)	35pF (max)	no used



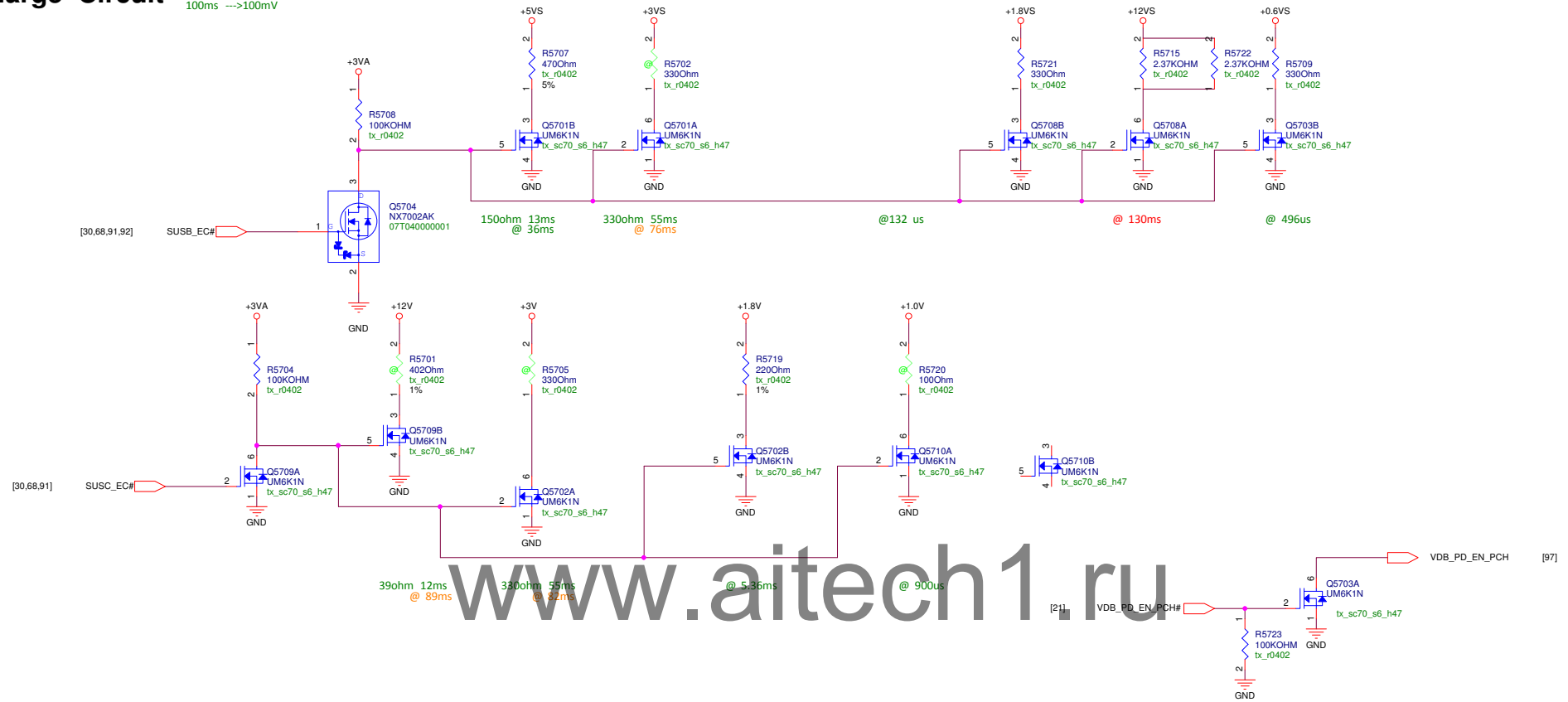
## FPC connector (for POGO PCB)



# Discharge Circuit

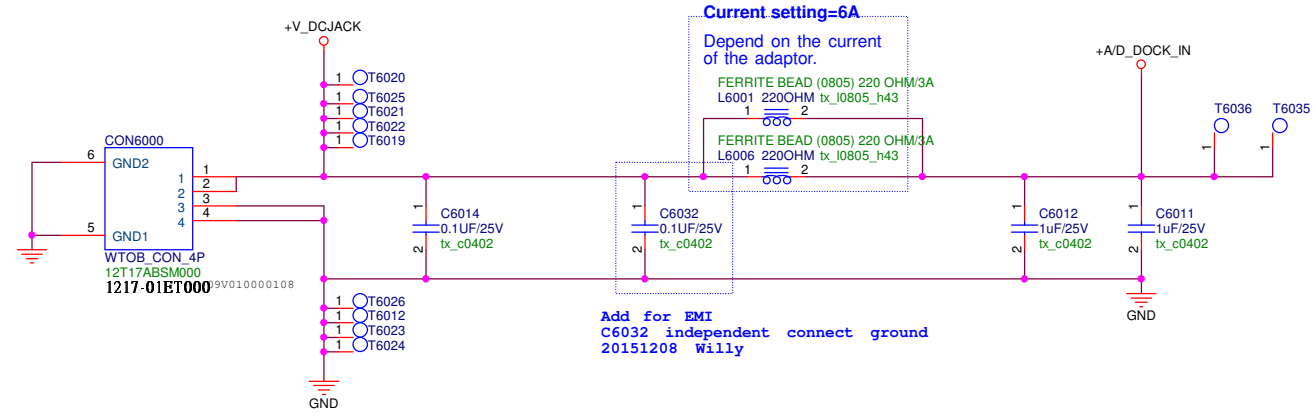
100ms ---->100mV

0402 1/16W min. resistor  
5V 400 OHM  
3V 144 OHM  
12V 2304 OHM



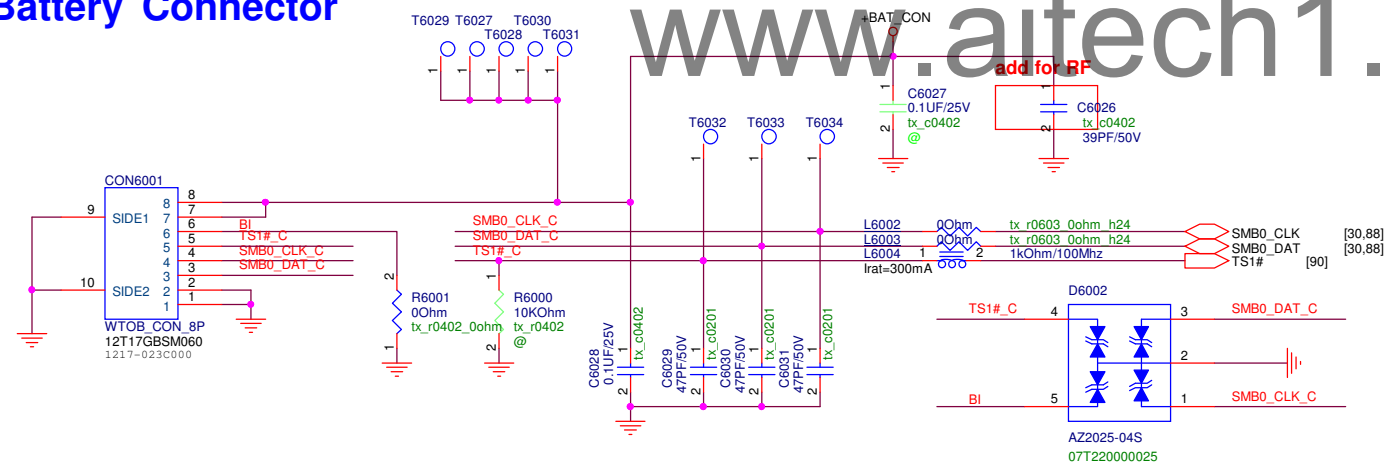
+1.0V	[7,91]	+0.6VS	[16,17,83]
+1.8V	[16,91]	+12VS	[91]
+3V	[25,91]	+1.8VS	[21,36,45,55,91]
+12V	[91]	+3VS	[3,4,20,21,22,23,24,30,32,36,40,41,44,45,50,51,53,55,56,62,70,91,92]
+3VA	[24,30,36,53,56,70,81,88,93,95,96,97]	+5VS	[36,55,56,80,91]

DC Jack WtoB CONN



- +VCC\_RTC to +VCC\_RTC [24,25,26,36]
- +3VA\_EC to +3VA\_EC [28,30,32,97]
- +3VA to +3VA [24,30,36,53,56,57,70,81,88,93,95]
- +5VA to +5VA [56,81]
- +1.0VSUS to +1.0VSUS [26,82]
- +1.8VSUS to +1.8VSUS [9,26,84]
- +3VSUS to +3VSUS [4,25,26,28,30,51,53,62,68,81,84,92,95]
- +5VSUS to +5VSUS [52,56,81,84,95,96]
- +12VSUS to +12VSUS [81,91]
- +3V to +3V [25,57,91]
- +12V to +12V [57,91]
- +1.8VS to +1.8VS [21,36,45,55,57,91]
- +3VS to +3VS [3,4,20,21,22,23,24,30,32,36,40,41,44,45,50,51,53,55,56,57,62,70,91,92]
- +5VS to +5VS [36,55,56,57,80,91]
- +12VS to +12VS [57,91]

Battery Connector



- +AC\_BAT\_SYS to +AC\_BAT\_SYS [45,80,81,82,83,88,97]
- +A/D\_DOCK\_IN to +A/D\_DOCK\_IN [89]
- +BAT\_CON to +BAT\_CON [88]
- +VCCORE to +VCCORE [5,80]
- +VCCGT to +VCCGT [6,80]
- +VCCSA to +VCCSA [7,80]
- +VCCIO to +VCCIO [3,7,9,91]

07T220000025	Vrwm ( Reverse Stand-Off Voltage )	CL ( Any I/O pin to GND )	Hawaii
0718-017D000	5.0V (max)	15pF (max)	V
0722-005C000	5.0V (max)	15pF (max) / 12 (typ)	V

PEGATRON

Title : DC\_DC/BAT CONN

Engineer: Willy\_Liao

Size  
B

Project Name  
GUAM

Rev  
0.0

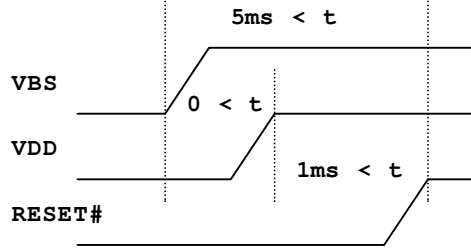
Date: Wednesday, March 15, 2017

Sheet 60 of 100

# TPM

VDD: Power the I/O buffers of the GPIO ports and the Host Interface  
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

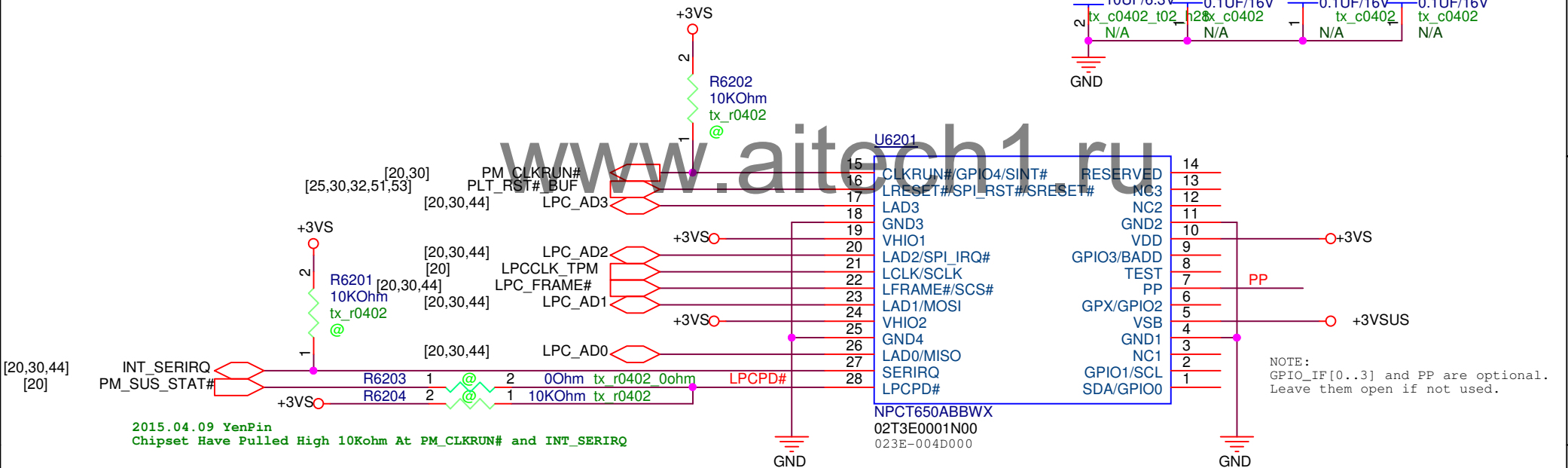
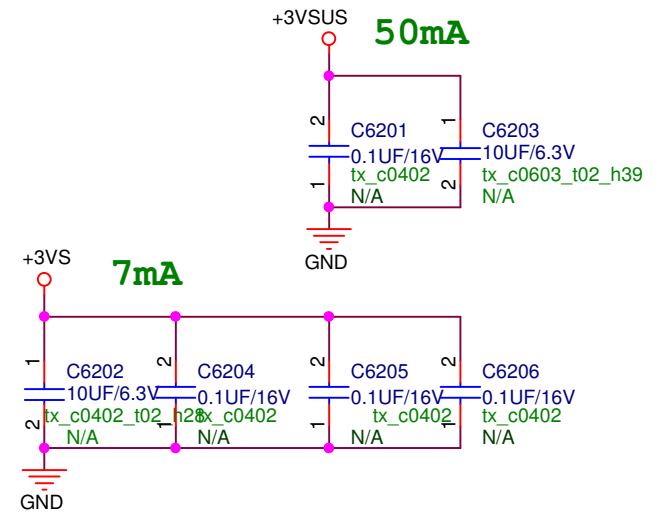
## TPM Power Sequence



NOTE: RESET# is LRESET#, SPI\_RST# or SRESET#.

### NOTE:

- 1) For TPM 1.2:  
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
- 2) For TPM 2.0:  
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
- 3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
- 4) RESET# must be asserted for at least 5 msec after VSB power-up.
- 5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
- 6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.



2015.04.09 YenPin  
Chipset Have Pulled High 10Kohm At PM\_CLKRUN# and INT\_SERIRQ

### NOTE:

- 1) The PP is an input signal with configurable polarity.
- 2) By default the PP functionality is disabled.

### Note:

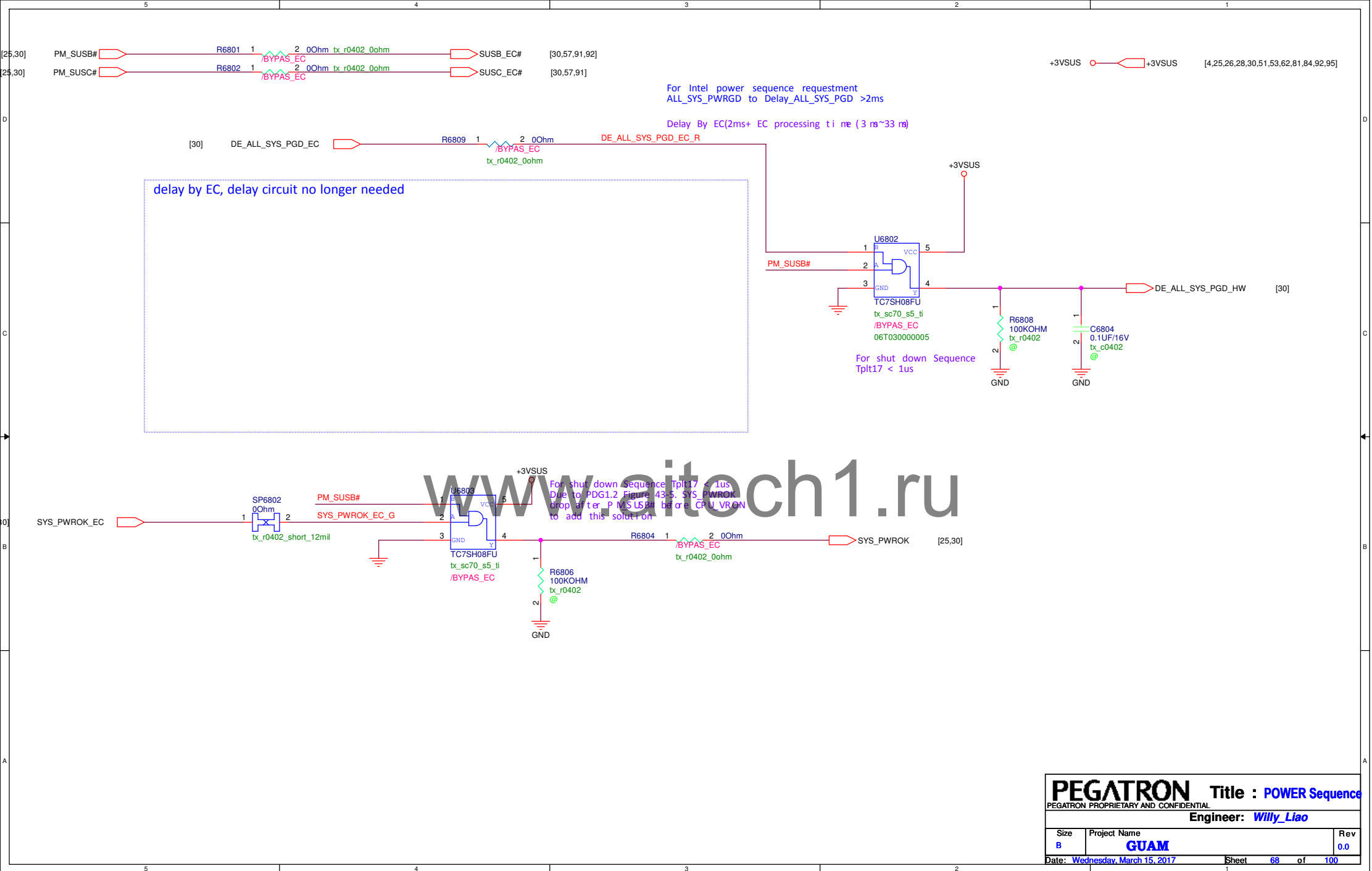
When LPCPD# functionality is not required, an internal pull-up resistor allows this pin to be left floating.

023E-003X000 TPM 2.0 F/W:1.3.0.1 FAB:Tower (ISRAEL)  
023E-0049000 TPM 2.0 F/W:1.3.0.1 FAB:TPSco (JAPAN)  
023E-004D000 TPM 2.0 F/W:1.3.1.0

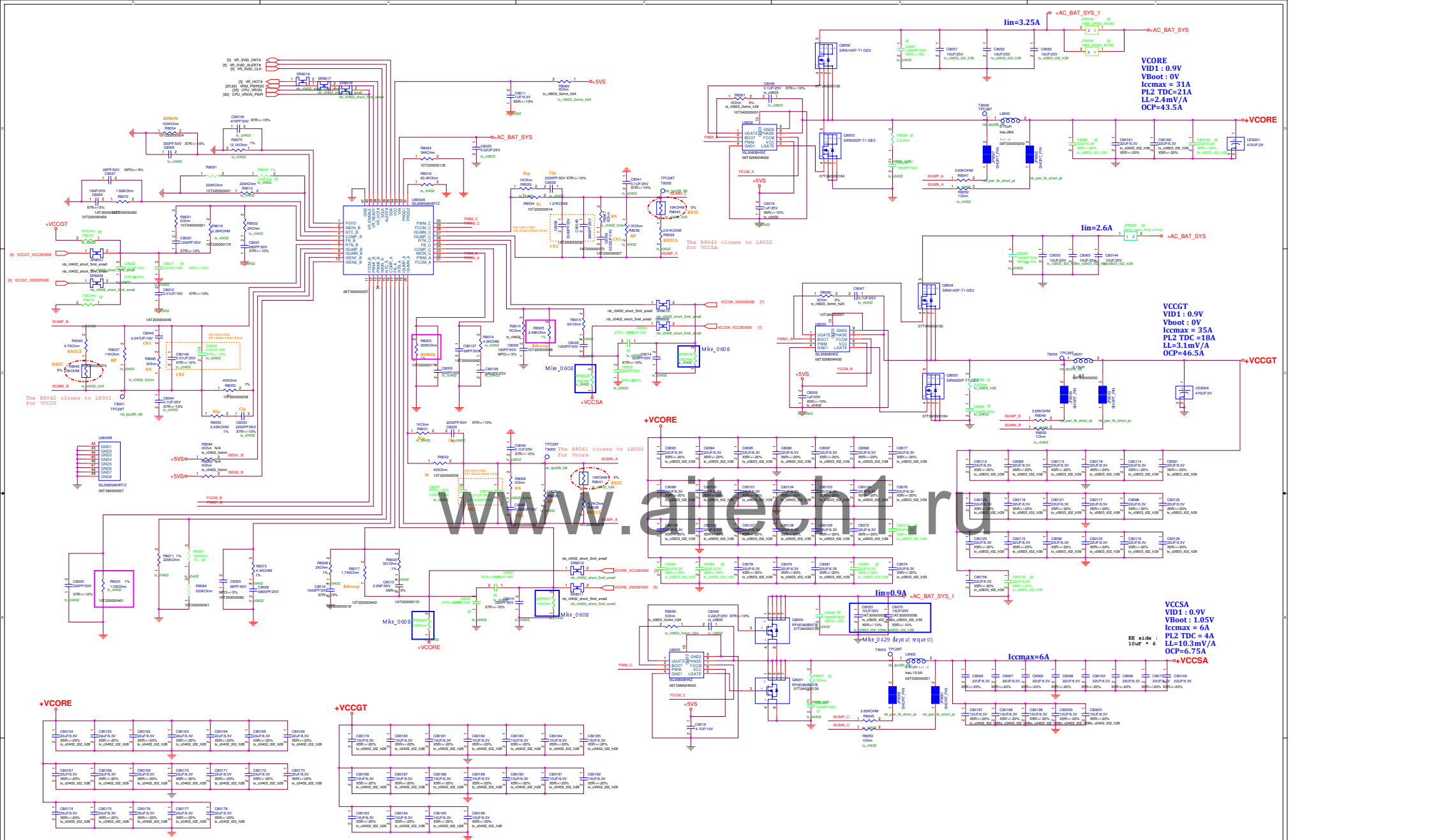
**PEGATRON** Title : **TPM**

Engineer: **Willy\_Liao**

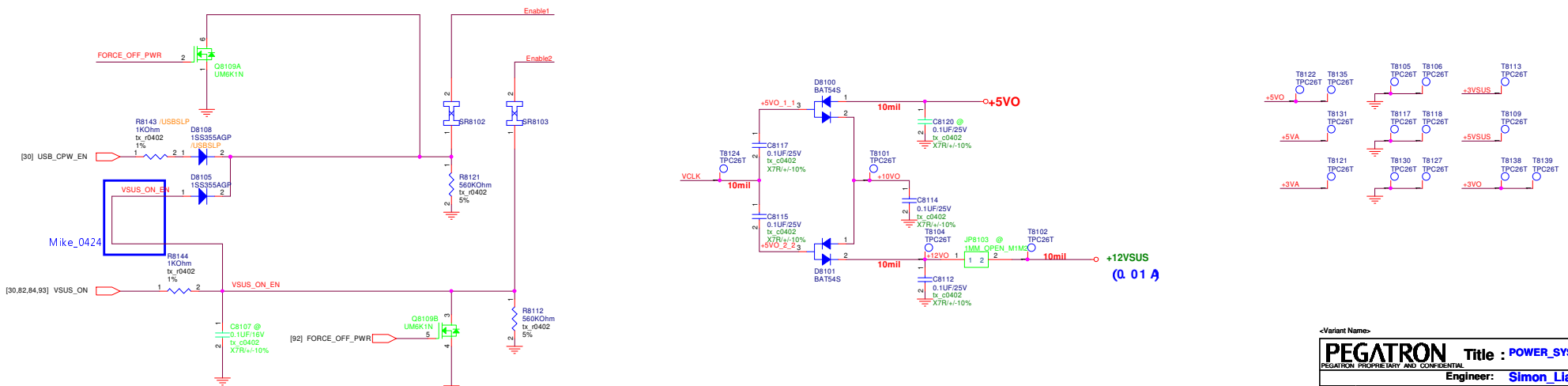
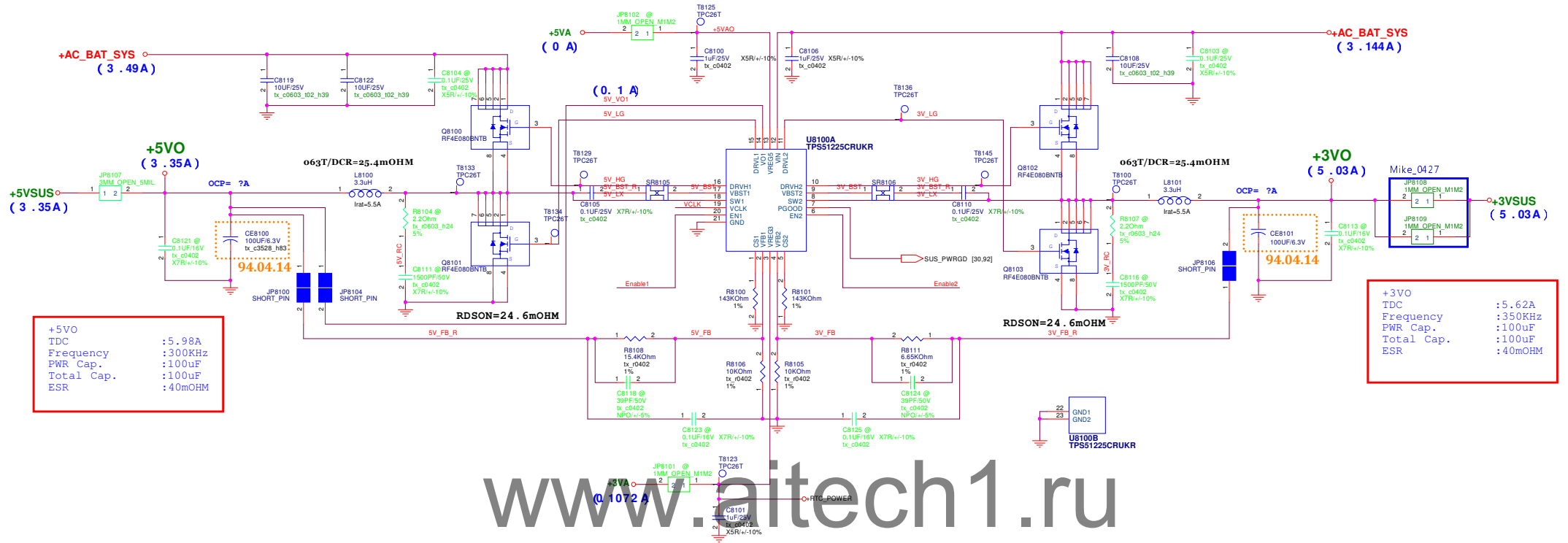
Size	Project Name	Rev
A	GUAM	0.0
Date: Wednesday, March 15, 2017	Sheet 62 of 100	







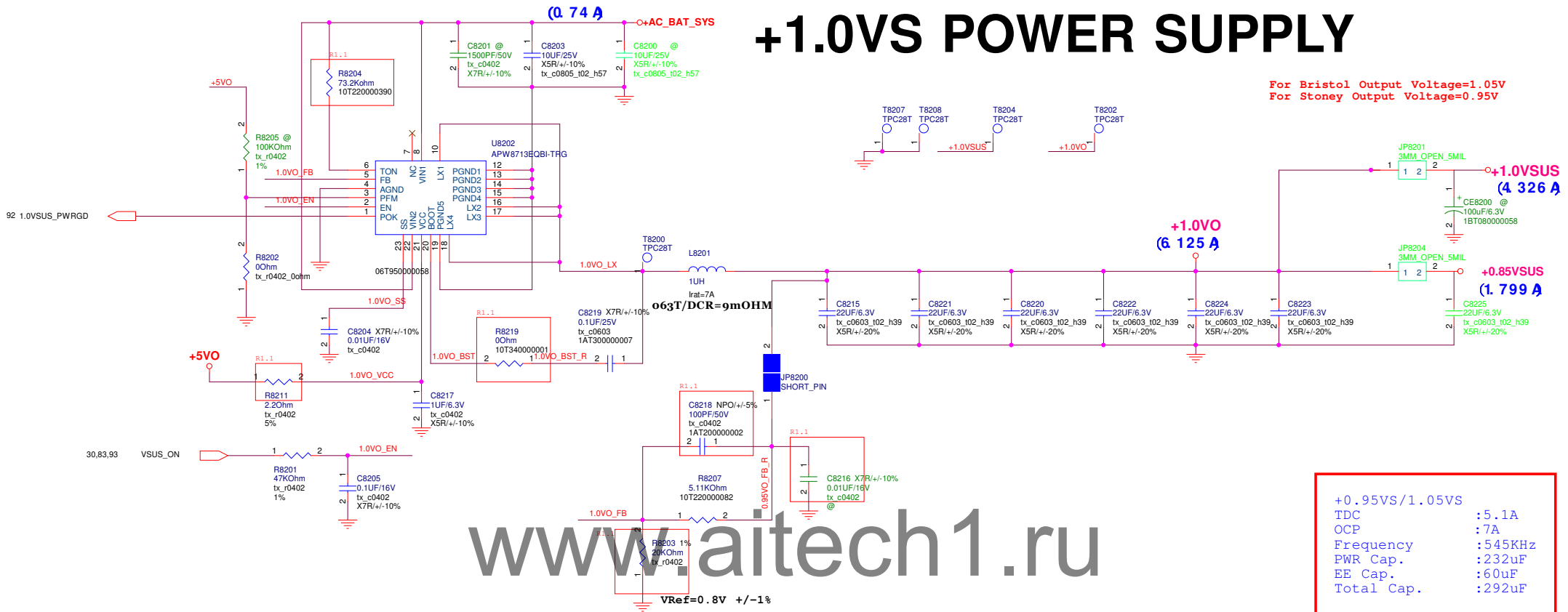
## +5V0 & +3V0 POWER SUPPLY





# +1.0VS POWER SUPPLY

For Bristol Output Voltage=1.05V  
For Stoney Output Voltage=0.95V



For Bristol R8207=6.2KOHM(10V220000088), Output Voltage=1.05V  
For Stoney R8207=3.74KOHM(10V2200000233), Output Voltage=0.95V

+0.95VS/1.05VS  
TDC :5.1A  
OCP :7A  
Frequency :545KHz  
PWR Cap. :232uF  
EE Cap. :60uF  
Total Cap. :292uF

<Variant Name>		
<b>PEGATRON</b> Title : +0.95VS/+1.0VS		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
Engineer: Simon Liao		
Size	Project Name	Rev
Custom	Guam	1.0
Date: Wednesday, March 15, 2017 Sheet 82 of 96		

330A  
500kHz

330A  
500kHz

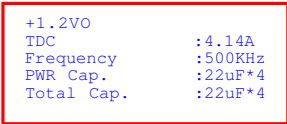
330A  
500kHz

330A  
500kHz

C8302  
RF4E080BNTB

C8307 @  
1500PF 50V  
tx c0402

RDSon=24.6mOhm

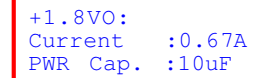


VID	Reference Voltage (V)
High	0.675 1%
Low	0.75 1%

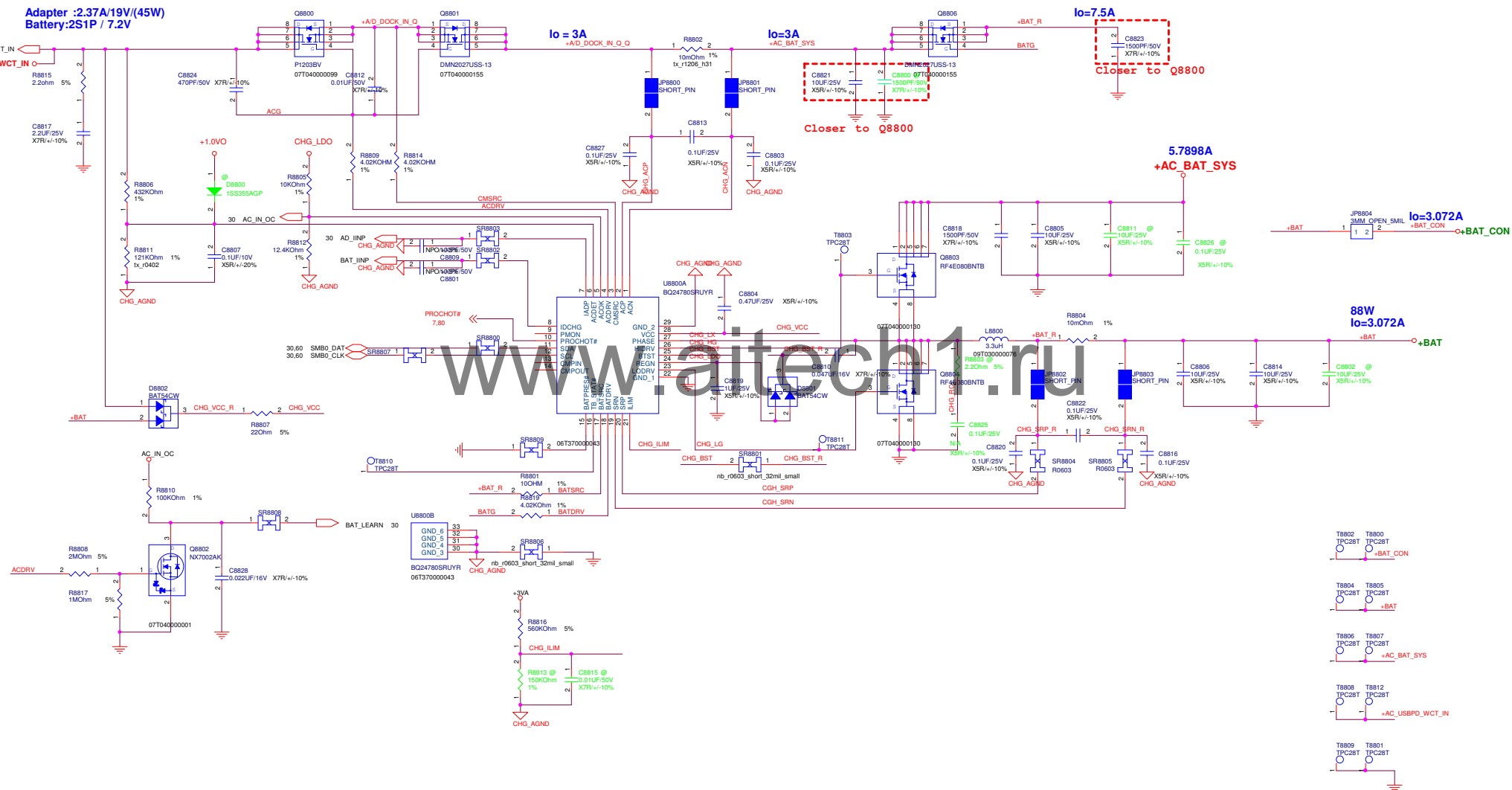
SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

**94.04.10 need to change**

## (Typ:1.816V ; Max:1.866V ; Min:1.767V)

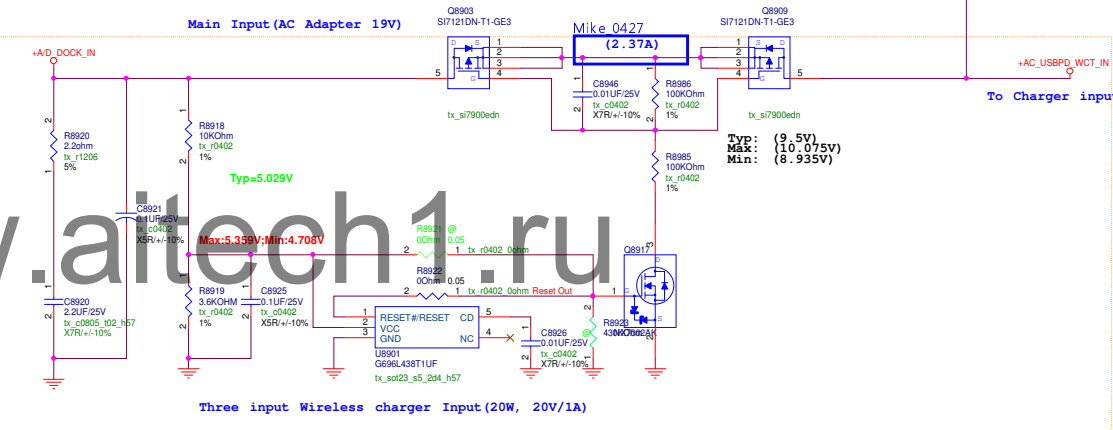
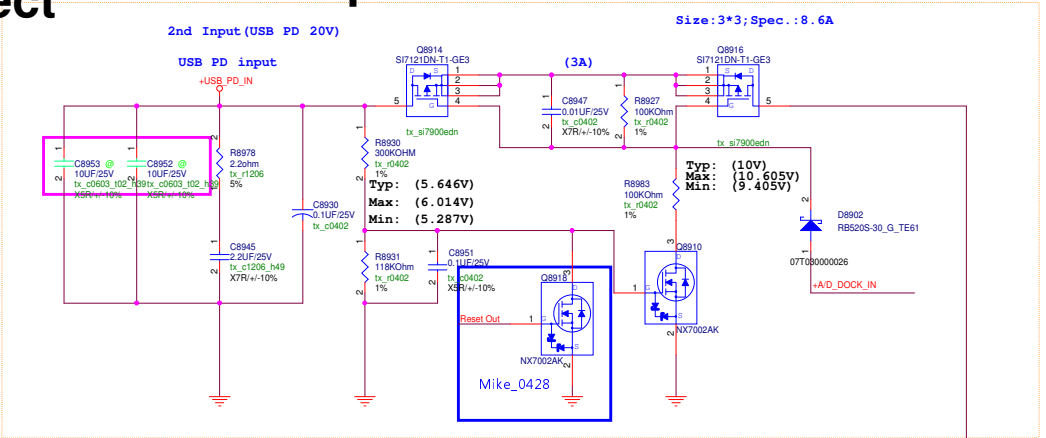
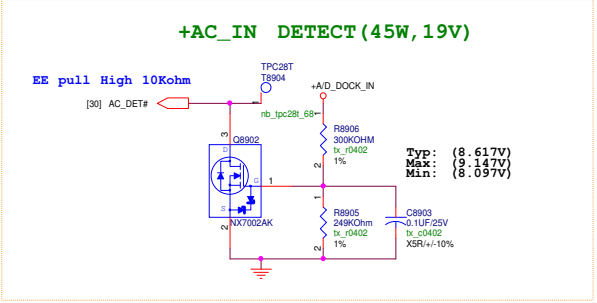
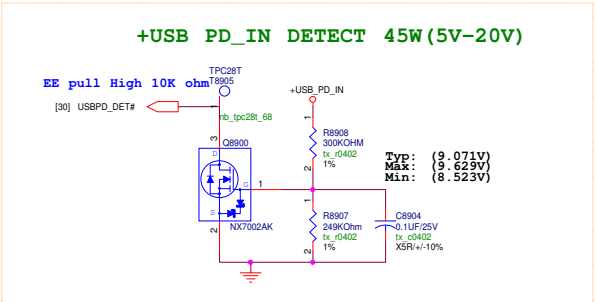


## BATTERY CHARGER



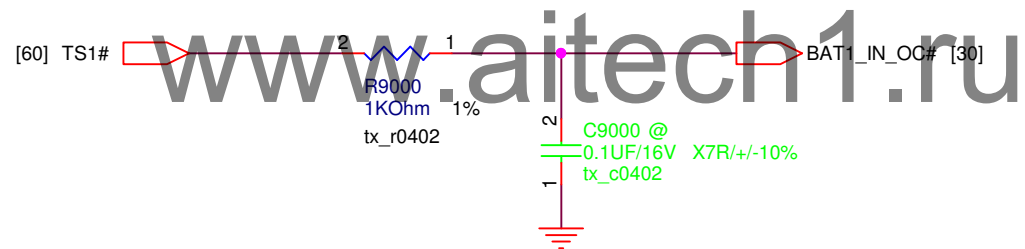
AC & USB\_PD & Wireless Charger Detect

3 Input switch Circuit



USBPD_DET#	AC_DET#	WCT_DET#	WCT_LEN	BQ24780S Charger EN DAT&CLK	DPM	Power Limit
0	0	0	L	H	AC_Adapter	45W*90%
0	0	1	L	H	AC_Adapter	45W*90%
0	1	0	L	H	USB_PD	45W*90%??
0	1	1	L	H	USB_PD	45W*90%??
1	0	0	L	H	AC_Adapter	45W*90%
1	0	1	L	H	AC_Adapter	45W*90%
1	1	0	L	H	WCT	20W*90%
1	1	1	X	X	X	X

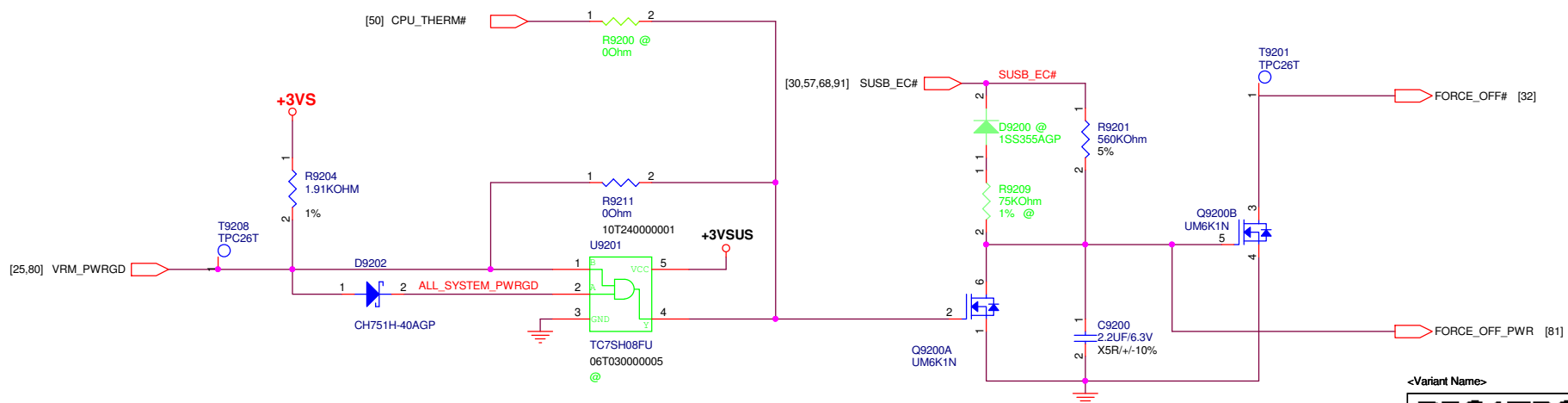
# BATTERY IN DETECT



<Variant Name>

<b>PEGATRON</b>		<b>Title :POWER_DETECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer: Simon_Liao</b>	
Size <b>A</b>	Project Name <b>Guam</b>		Rev <b>1.0</b>
Date: <b>Wednesday, March 15, 2017</b>		Sheet <b>90</b> of <b>96</b>	

Figure 10 consists of two circuit diagrams for test fixtures SR9101 and SR9100. Both diagrams show a probe (T9100 for SR9101, T9110 for SR9100) connected to a short circuit (5mil\_small) and a signal line (SUSC\_EC# or SUSB\_EC#). The probe is also connected to a power line (SUSC# PWR or SUSB# PWR). The diagrams are labeled with the probe model (T9100 or T9110) and the short circuit length (5mil\_small).

[illegible]

<b>PEGATRON</b>		Title : <b>POWER_PROTECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Simon_Liao</b>	
Size <i>Custom</i>	Project Name <b>Guam</b>		Rev <b>1.0</b>
Date:	<b>Wednesday, March 15, 2017</b>	Sheet	<b>92 of 96</b>



+AC\_USBDPD\_WCT\_IN > +AC\_USBDPD\_WCT\_IN 88  
+AC\_BAT\_SYS > +AC\_BAT\_SYS 80,81,83,87,88  
+BAT\_CON > +BAT\_CON 88  
+BAT > +BAT 88  
+5VA > +5VA 81  
+3VA > +3VA 81,88  
+5VO > +5VO 81,83,91  
+3VO > +3VO 81,82,84,86,91

+1.8VO > +1.8VO 84  
+1.2VO > +1.2VO 83,91  
+1.0VO > +1.0VO 82  
+0.6VO > +0.6VO 83  
+12VSUS > +12VSUS 81,91  
+5VSUS > +5VSUS 81  
+3VSUS > +3VSUS 81,92

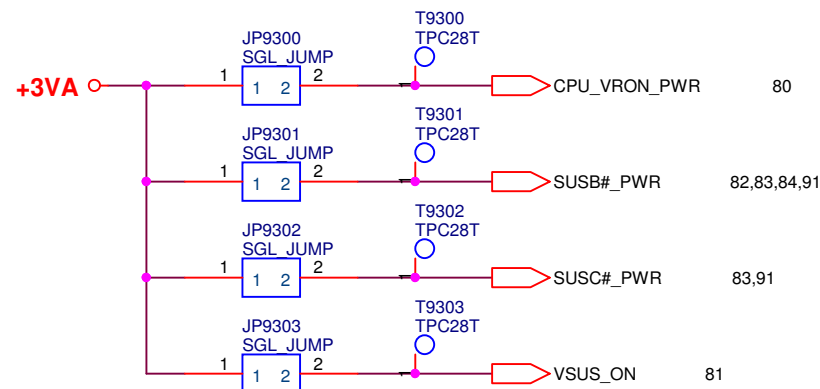
+3V > +3V 91

+1.2V > +1.2V 83  
+12VS > +12VS 91  
+5VS > +5VS 80,87,91  
+3VS > +3VS 80,91,92

+0.6VS > +0.6VS 83

+VCORE > +VCORE 80

## FOR POWER TEST



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<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_SIGNAL</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Size Custom		Project Name <b>Guam</b>	
Date: <b>Wednesday, March 15, 2017</b>		Rev 1.0	
Sheet <b>93</b>		of <b>96</b>	



# ANX7428

Connect to DP Source

Connect to USB3.0 signals

M\_SDA/GPIO\_5 pin:  
Connect to AP/CPU/Charge IC as a charge mode indicator.  
Logic 0: Fast Charger Mode, charge voltage > 5V and charge current >= 1.5A.  
Logic 1: Normal Charger Mode, charge voltage = 5V and charge current < 1.5A.

## I2C Address Selection:

I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

I2C\_ADR\_1 and I2C\_ADR\_0 pin:  
1. The I2C address is determined approximately 500ns after RESET\_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.  
2. There are internal pull-down resistors on I2C\_ADR\_0 and I2C\_ADR\_1 pins.  
3. If external pull-up resistor is not populated, the I2C\_ADR\_0 or I2C\_ADR\_1 is logic 0.  
4. If external pull-up is populated, the I2C\_ADR\_0 or I2C\_ADR\_1 is logic 1.

The DVDD\_IO can be power supplied by 1.8V ~ 3.3V:  
If AP's IO type is 1.8V, select 1.8V power for DVDD\_IO;  
If AP's IO type is 3.3V, select 3.3V power for DVDD\_IO.

V5\_VCONN is the power source for VCONN(UTC\_B5\_CC2 or UTC\_A5\_CC1).  
Please make sure:  
1) VCONN Voltage range [4.75V, 5.5V]  
2) VCONN Minimum power is 1W. If DP Alternate Mode is supported, VCONN power is up to 1.5W.  
Reverse voltage protection is required.  
It might be necessary to add a diode to protect the power supply.  
Requirement of Q3:  
1) Id >= 500mA (Vgs = - 4.5V).  
2) Ron < 120 mOhm (Vgs = - 4.5V).  
3) Max Vds >= -10V.

Connect to USB Type-C connector

INTP\_OUT pin: interrupt output.  
Connect to AP or CPU.  
Enable MCU interrupt. Set EX1=1

CABLE\_DET pin: Connect to AP or CPU.  
Logic 1: USB Type-C cable plug detected.  
Logic 0: USB Type-C cable unplugged detected.

Note:  
1. Set R21 = 100K, C15 = 22nF to filter the short high toggle pulse in DRP mode when cable is unplugged in ES chip.  
2. Set R21 to 0R, C15 to DNP when this is fixed in CS chip.

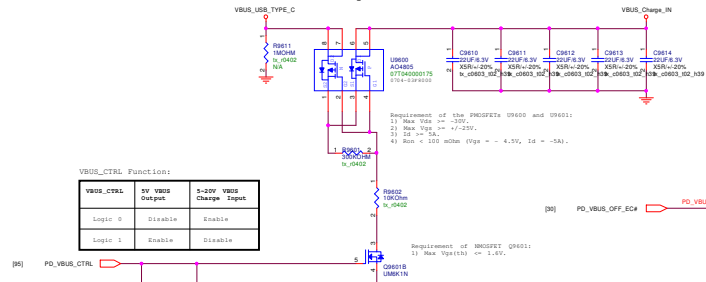
PWR\_EN pin:  
Controlled by AP or CPU  
Logic 1: to power up the chip.  
Logic 0: to power down the chip.

<Variant Name>

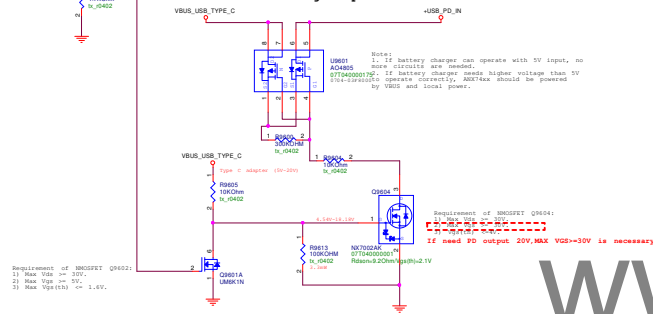
## VBUS Control

Optional:  
If PMIC can detect VBUS presence and disable/enable VBUS,  
the VBUS control circuit can be removed.

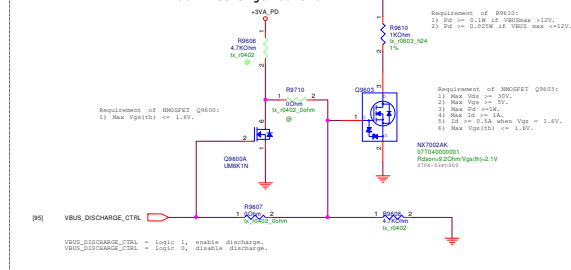
### 5V VBUS Output Control



### 5-20V VBUS Charge Input Control

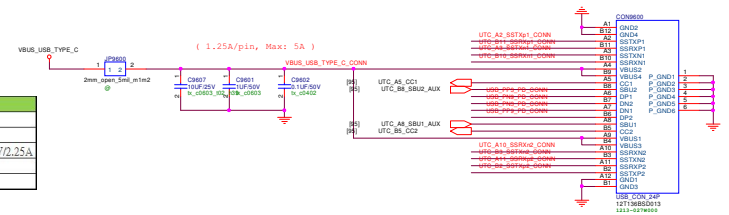


### VBUS Discharge Control



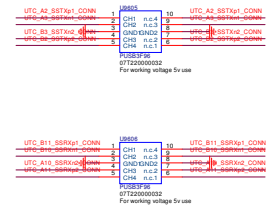
## USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SRU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SRU2	D+	D-	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1



USB TYPE C features	On Guam
CC logic	Yes
USB data transfer	ANX7428: USB 3.1 Gen1 (5Gbit/s), SOC: 3.0
Power Delivery	5V/2.25A (Cannot charge when dead battery), 12V/2.25A, 20V/2.25A
Support Power	5V/1.5A
DisplayPort Alternative Mode	ANX7428: DP1.3, SOC: DP1.3

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Part Number	V <sub>revm</sub> (Reverse Stand-Off Voltage)	CL (Any I/O pin to GND)	Hawaii
07T220000032	5.0V (max)	0.65pF (max) / 0.5pF (typ)	V
07T220000032	5.5V (max)	0.6pF (max) / 0.5pF (typ)	V
07T220000032	5.0V (max)	0.6pF (max) / 0.4pF (typ)	no used
07T220000032	5.0V (max)	0.8pF (max)	no used

Part Number	V <sub>revm</sub> (Reverse Stand-Off Voltage)	CL (Any I/O pin to GND)	Hawaii
07T180000052	24V	50pF (max) / 42.5pF (typ)	V

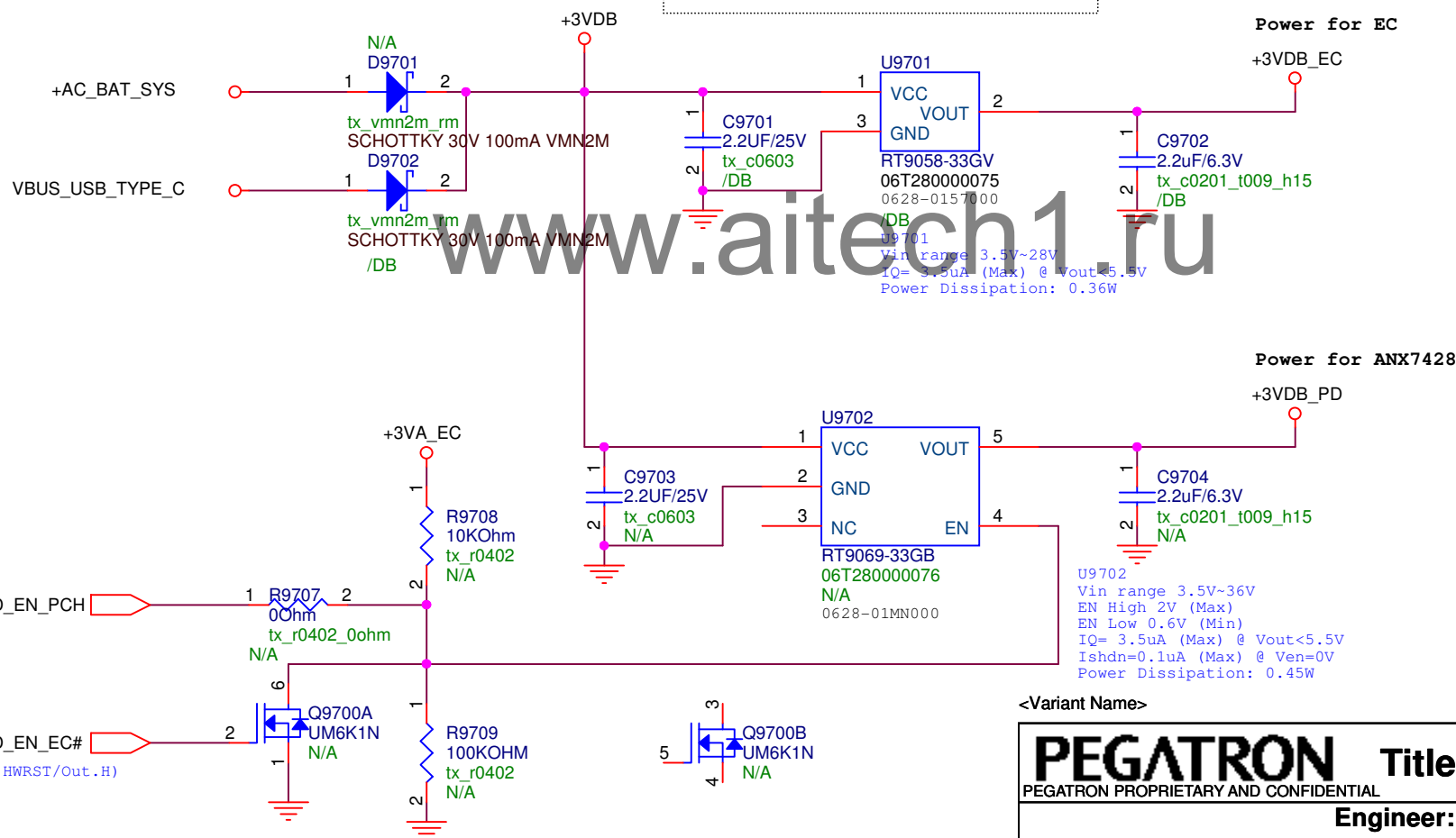
## Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C		VBUS_USB_TYPE_C	[28,95,96]
+AC_BAT_SYS		+AC_BAT_SYS	[45,80,81,82,83,88]
+3VDB_EC		+3VDB_EC	[30]
+3VDB_PD		+3VDB_PD	[95]
+3VA_EC		+3VA_EC	[28,30,32]

Requirement of U1:

- 1)  $V_{in}$  range: 4V-30V.
- 2)  $V_{out}$ : EC's operating voltage +  $V_f$  of D1.
- 3) Output current  $\geq$  EC's operating current.



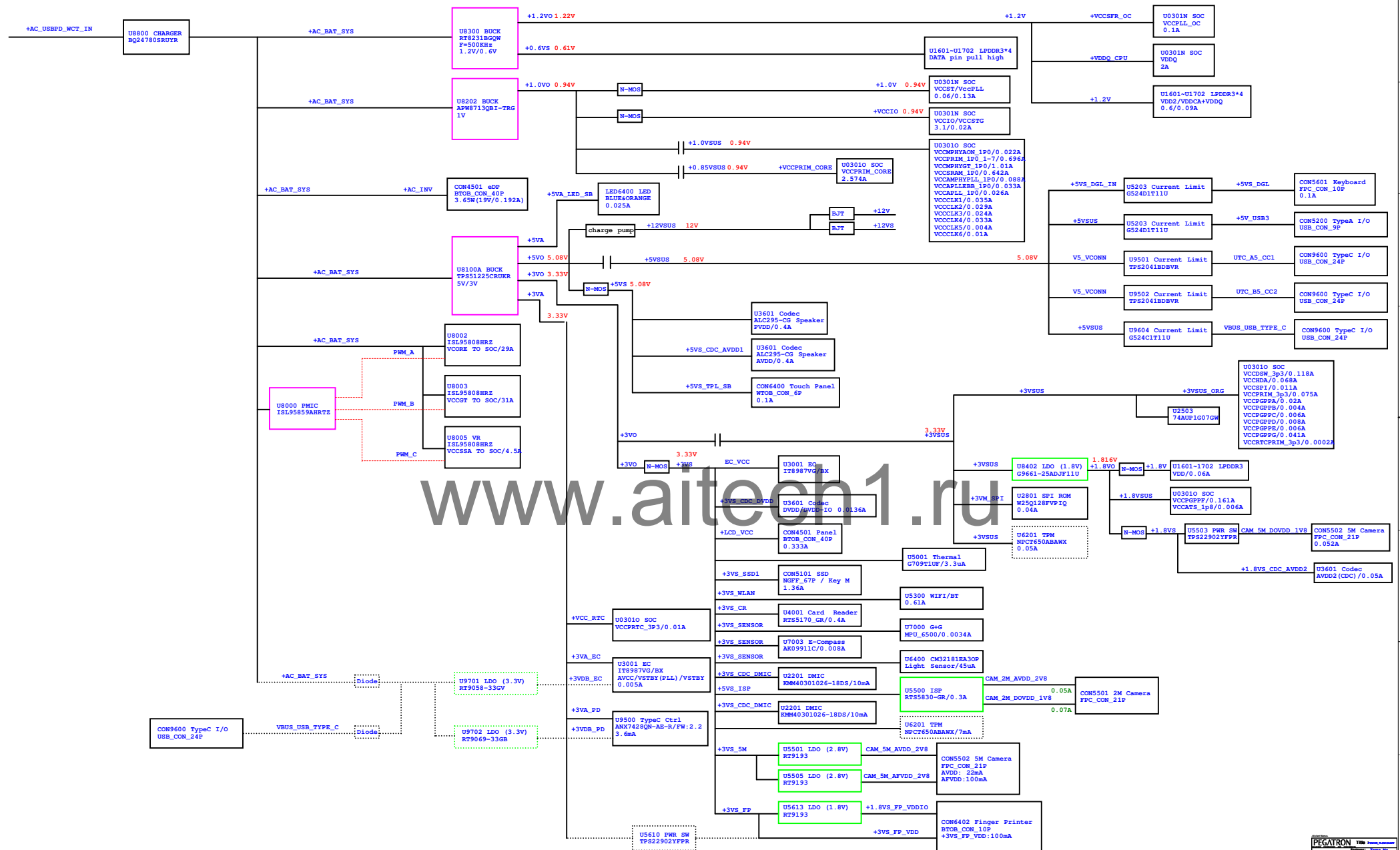
<Variant Name>

# PEGATRON

**Title :** Dead Battery

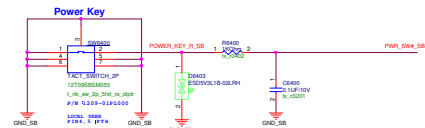
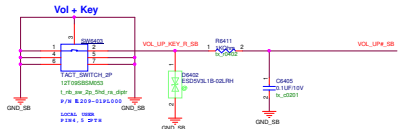
**Engineer:** **Willy Liao**

Size A	Project Name <b>GUAM</b>	Rev 0.0
Date:	Wednesday, March 15, 2017	Sheet 97 of 100

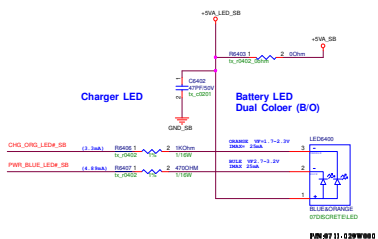


# IO Board CONN

(Remove HOME\_KEY#)

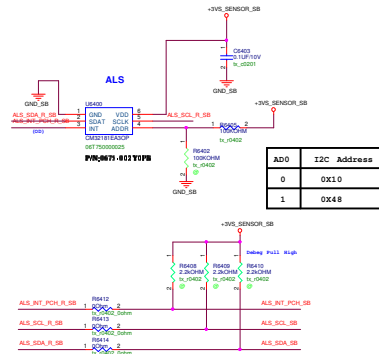


## LED

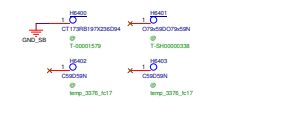


LED	Blue	Orange	TRD
AC mode	Fully Charge	Charging	N/A
DC mode	100%-110%	90%-110%	10%-10%

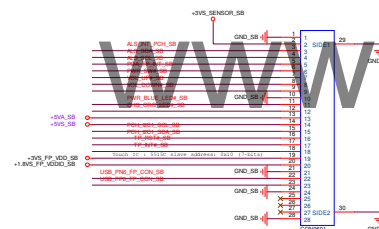
## ALS



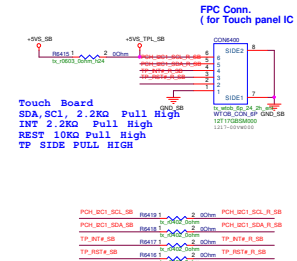
Screw Hole / Tooling Hole  
(for hawaii\_sub\_pcb\_1002)



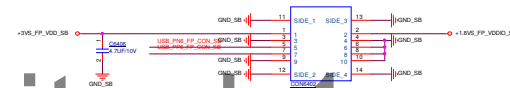
FPC connector  
(for Main PCB)



## Touch board



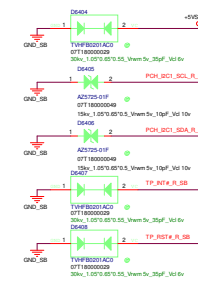
## Finger Printer



Close to CON6402

10K

Close to CON6400



Close to CON6402

